Code No: RT31045 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November - 2015

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is the radiation resistance of half wave dipole antenna?	[3M]
	b)	What are the far field conditions for an antenna?	[3M]
	c)	Discuss the merits and demerits of zoned antennas.	[4M]
	d)	Calculate PLF (dB) when polarization of incoming wave is perfectly matched to polarization of Rx antenna.	[4M]
	e)	Name the parasitic elements used in Yagi uda array. Explain their significance in array.	[4M]
	f)	In which frequency band Tropospheric scattering is used.	[4M]

PART -B

2	a)	With the help of neat diagrams explain the principle of radiation mechanism in antennas.	[8M]
	b)	A source has a constant power pattern limited to top half of the hemisphere only. Find its directivity and effective area.	[8M]
3	a)	The normalized radiation intensity of an antenna is rotationally symmetric in ϕ and it is represented by $U = \begin{cases} 1 & 0 \le \theta < 30^0 \\ 0.5 & 30^0 \le \theta < 60^0 \\ 0.1 & 60^0 \le \theta < 90^0 \\ 0 & 90^0 \le \theta < 180^0 \end{cases}$ What is the directivity (above isotropic) of antenna in dB?	[8M]
	b)	Derive the relationship between effective aperture area and gain of antenna.	[8M]
4	a)	Write short notes on: i) Collinear arrays ii) Binomial arrays and iii) Scanning arrays.	[8M]
	b)	Draw the radiation pattern of 8 – isotropic elements fed in phase, spaced $\lambda/2$ apart with the principle of pattern multiplication.	[8M]

5	a)	Derive the expression for pitch angle to get circularly polarized radiation pattern for a helical antenna, operating in broadside mode and sketch its pattern.	[8M]
	b)	Compare the requirements and radiation characteristics of resonant and non-resonant radiators?	[8M]
6	a)	List out the differences between active and passive corner reflectors.	[8M]
	b)	With reference to paraboloids, explain the following: i) f/D ratio ii) Spill over and aperture efficiency iii) Front to back ratio iv) Types of feeds.	[8M]
7	a)	Describe briefly the salient features of ground wave propagation.	[6M]
	b)	What should be the polarization of EM wave for the ground wave propagation? Justify.	[6M]
	c)	Explain the term" wave tilt of surface waves".	[4M]

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Code No: RT31045 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) What is the difference between directive gain and gain of antenna? [4M]

b) A transmitting antenna radiates 251W isotropically. A receiving antenna, located 100m away from the transmitting antenna, has an effective aperture of 500cm^2. Determine the total power received by the antenna. [4M]

c) For an 8ft (2.4m) parabolic dish antenna operating at 4GHz, What is the minimum distance required for far field measurement? [4M]

d) A wave traveling normally out of the page (toward the reader) has two linearly polarized components $E_x = 2\cos\omega t$ [4M]

$$E_y = 3\cos(\omega t + 90^\circ)$$

What is the axial ratio of the resultant wave?

e) What is the skip zone of a radio wave? [3M]

f) How do raindrops affect radio waves? [3M]

PART -B

2 a) What are the differences between transmission line and dipole antenna? [4M]

b) Sketch and comment on the current distributions and radiation patterns of vertical antennas of length λ/2, λ, 3λ/2, 2λ. [8M]

c) Write short notes on antenna field zones. [4M]

3 a) The power radiated by a lossless antenna is 10W. The directional characteristics of the Antenna are represented by the radiation intensity of [8M]

$$U = B_0 \cos^3\theta \left(\frac{W}{unit\ \ solid\ angle}\right) 0 \le \theta \le \frac{\pi}{2};\quad 0 \le \phi \le 2\pi .$$

Find B_0, Maximum radiation intensity and Maximum power density (W/m^2) at a distance of 1000m (assume far field distance).

b) A short antenna of height $h = l/2$ is mounted on a conducting plane. Show that its radiation resistance is one-half that of a short dipole antenna of length l and carrying the same current. [8M]

4 a) Explain the need and configuration of a folded dipole antenna. Sketch its radiation pattern and compare its characteristics with those of a simple half wave dipole. [8M]

b) Obtain the expression for the beam width of broadside and end-fire array and compare them. [8M]

5 a) Explain the salient features of Microstrip Antennas. [8M]

b) What are the advantages and limitations of Microstrip antennas? [8M]

6 a) Explain the principle of formation of images in an active corner reflector antenna. Hence sketch the image formation for a 90^o corner reflector. Obtain array factor for 90^o corner reflector. [8M]

b) What is the principle of equality of path length? How is it applicable to Horn antennas? Obtain an expression for the directivity of a pyramidal horn in terms of its aperture dimensions. [8M]

7 a) List out the modes of propagation and their frequency ranges for radio waves. Show that an approximate estimate for the magnitude of electric field strength at VHF and above is given by $\left(\frac{240I\pi h_1 h_2}{\lambda d^2}\right)$ [8M]

where I - current in the λ/2 transmitting aerial
h1, h2 - heights of Tx and Rx antennas
d - direct distance between aerials
λ - wavelength.
Specify the assumptions made for the validity of the above expression.

b) Write a short notes on: [8M]
i) MUF
ii) Virtual Height
iii) Wave tilt
iv) Multihop Transmission.

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Code No: RT31045 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is the effect of antenna's sidelobes and backlobes on its gain?	[3M]
	b)	Calculate half power beamwidth for a hertzian dipole.	[4M]
	c)	What is the directivity of isotropic antenna?	[3M]
	d)	What are the advantages of cassegrain feed in parabolic antenna?	[4M]
	e)	In which frequency range ground wave propagation is effective. Why?	[4M]
	f)	What is the difference between broad-side array and end-fire array?	[4M]

PART -B

2	a)	An infinitesimal electric dipole is centered at the origin and lies along z-axis. Find the far–zone electric and magnetic fields radiated.	[8M]
	b)	An infinitesimal electric dipole is centered at the origin and lies on the x-y plane along a line which is at an angle of 45^0 with respect to the x-axis. Find the far –zone electric and magnetic fields radiated.	[4M]
	c)	Compare monopole antennas and dipole antennas.	[4M]
3	a)	The normalized radiation intensity of a given antenna is given by $U = \sin\theta \sin\phi$. The intensity exists only in the region $0 \le \theta \le \pi, 0 \le \phi \le \pi$ and it is zero elsewhere. Find azimuthal and elevation plane half power beam widths (in degrees).	[3M]
	b)	Derive the relation between directivity and beam solid angle.	[8M]
	c)	The Electric field of a linearly polarized electromagnetic wave given by $E_i = a_x E_0(x, y) e^{-jkz}$ is incident upon a linearly polarized antenna whose electric field polarization can be expressed as $E_a = (a_x + a_y) E(r, \theta, \phi)$. Find polarization loss factor (PLF).	[5M]
4	a)	Explain the effects of uniform and non-uniform amplitude distributions in array?	[8M]
	b)	Explain how to select current excitations in an array to avoid sidelobes in radiation pattern?	[8M]

5 a) Describe the characteristics of long wire travelling wave antennas and sketch their patterns for different lengths. [8M]

b) What are the advantages of Rhombic antenna over a single wire antenna? List out the design equations associated with a Rhombic antenna. [8M]

6 a) With neat set up, explain the absolute method of measuring the gain of an antenna. [8M]

b) Discuss about Dielectric and metal Lens Antennas and their applications. [8M]

7 a) Derive the relationship between MUF and critical frequency. [8M]

b) Discuss experimental determination of virtual heights and critical frequencies. [8M]

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Code No: RT31045 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015

ANTENNAS AND WAVE PROPAGATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) What kind of antenna polarizations must be selected to avoid probability of interference between 2 co-channel radio links? [3M]

b) What is the advantage of using helical antenna over straight wire antenna? [4M]

c) In a uniform linear array, four isotropic radiating elements are spaced λ/2 apart. What is the required progressive phase shift between the elements for forming the main beam at 60^0 off the end-fire? [4M]

d) Calculate PLF (dB) when polarization of incoming wave is orthogonal to polarization of Rx antenna. [4M]

e) What three main factors determine the amount of refraction in the ionosphere? [3M]

f) After the radiation field leaves an antenna, what is the relationship between the E and H fields with respect to (a) phase and (b) physical displacement in space? [4M]

PART -B

2 a) Define the terms: [4M]
i) Effective length
ii) Effective aperture area.

b) Calculate effective length and effective aperture area of antenna whose radiation resistance is 73 ohms. [6M]

c) Derive the expression for power radiated and find the radiation resistance of a half wave dipole? [6M]

3 a) Calculate half power beam width when $E = \frac{\cos\left[\frac{\pi(\cos\theta+1)}{4}\right]e^{-jkr}}{r} \quad 0 \le \theta \le \pi$ [3M]

b) Define reciprocity theorem and prove it in case of antenna system. [8M]

c) What is the maximum effective aperture of a microwave antenna which has a directivity of 900? [5M]

4 a) Derive the expression for the far field pattern of an array of 2 – isotropic point sources of [8M]
i) Equal amplitude and phase
ii) Equal amplitude and opposite phase
iii) Unequal amplitude and any phase.

||''|'''|''|'|''''||

b) Find the radiation pattern of linear array of 4 isotropic sources spaced $\lambda/2$ apart. And sketch it. The excitations of sources are in phase and amplitude ratio 1:3:3:1. [8M]

5 a) Sketch the typical geometry of a helical antenna radiating in axial mode. List out all its parameters and basic characteristics. Write the expressions for HPBW, BWFN, directivity and axial ratio. [8M]

b) Compare the characteristics of Hertzian dipole and Hertzian Loop antenna. [8M]

6 a) What is radio horizon and optical horizon? Show that radio horizon is about 1.33 times the optical horizon. [8M]

b) What is the density of free electrons in the ionospheric layer at critical frequency of 1.3 MHz? [4M]

c) Explain the Gain comparison method for measuring the gain of an antenna. [4M]

7 a) Describe any two types of fading normally encountered in radio wave propagation. How are the problems of fading overcome? [8M]

b) Determine the change in the electron density of E-layer when the critical frequency changes from 4 MHz to 1 MHz between mid - day and sun-set. [8M]

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Code No: RT31043 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November - 2015

CONTROL SYSTEMS

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
(Normal and semi & polar graph sheets are to be supplied)

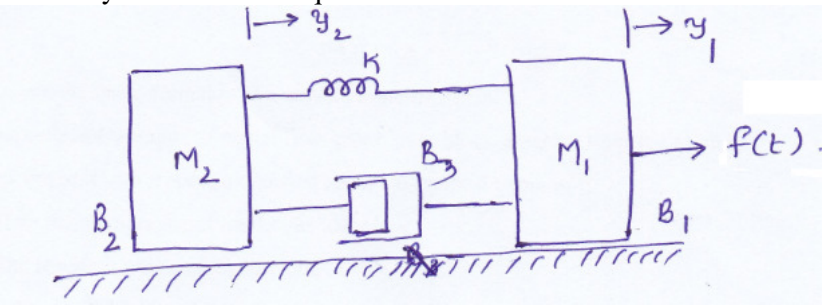
*****

PART –A

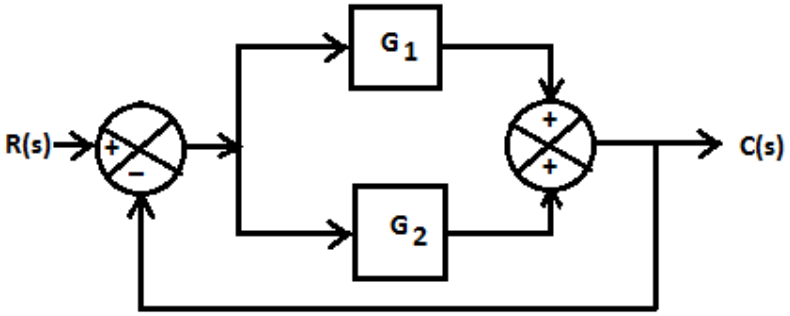
1	a)	What are the basic elements of a control system?	[3M]
	b)	Explain the advantages of signal flow graph over block diagram representation.	[4M]
	c)	Draw the unit step response of a first order system and explain.	[4M]
	d)	Explain the advantages of root locus technique.	[4M]
	e)	Define resonant peak and bandwidth.	[4M]
	f)	What is meant by Diagonalization?	[3M]

PART -B

2	a)	Write short notes on controlled variable and manipulated variable.	[4M]
	b)	Write the force equations of the linear translational system shown in figure. Draw the equivalent electrical network using force-voltage Analogy, with the help of necessary mathematical equations.	[8M]



	c)	What is meant by unity feedback control systems? Explain.	[4M]
3	a)	Draw the signal flow graph for the block diagram below and then obtain the transfer function C(s)/R(s) using Mason's gain formula.	[8M]



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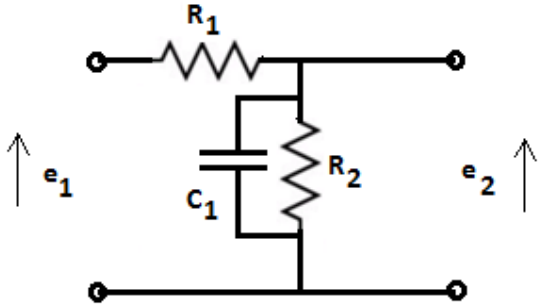
b) Obtain the transfer function $E_2(s)/E_1(s)$ for the electrical circuit below by representing the circuit into a block diagram and using block diagram algebra. [8M]



4 a) Explain the effect of PID control action on the performance of a second order system [6M]

b) Determine the step, ramp and parabolic error constants of the following unity feedback control system whose open loop transfer function is given by [10M]

$$G(s) = \frac{500}{(1+5s)\ (1+10s)}.$$

5 a) Using Routh-Hurwitz criterion, determine the stability of the closed loop system that has the following characteristic equation and also determine the number of roots that are in the right half s-plane and on the imaginary axis $s^4 + s^3 + 3s^2 + 2s + 5 = 0$. [7M]

b) Find the angles of departure and arrival for all complex poles and zeros of the open loop transfer function of $G(s)H(s) = \frac{K(s^2+3s+5)}{s(s^2+4)}, K > 0$. [9M]

6 a) Find resonant peak, resonant frequency and bandwidth of the unity feedback system whose open loop transfer function is as follows: $G(s) = \frac{0.5}{(s^2+3s+2)}$. [8M]

b) The characteristic equation of a linear control system is given below: [8M]

$$s^2 + 3s + 2 + K = 0\ .$$

Using Nyquist Stability Criterion, determine the range of K for the system to be stable.

7 a) Draw the electrical circuit diagram that represents the Lead-Lag Compensator and explain in detail. [8M]

b) Determine the state and output equations in vector matrix form for the system whose transfer function is given by $G(s) = \frac{(s+3)}{s(s^2+3s+2)}$. [8M]

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Code No: RT31043 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015

CONTROL SYSTEMS

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
(Normal and semi & polar graph sheets are to be supplied)

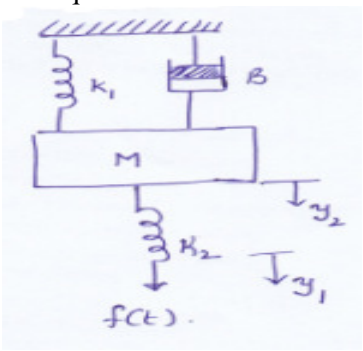
*****

PART –A

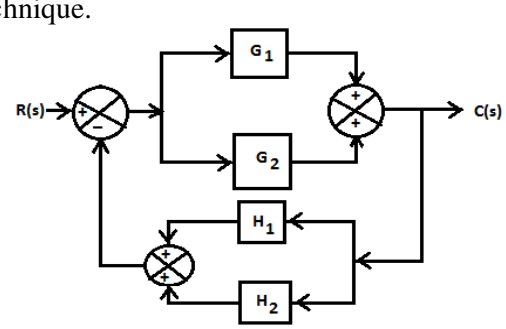
1	a)	What is meant by open loop control system?	[3M]
	b)	Describe the Mason's gain formula.	[4M]
	c)	Draw the unit impulse response of a first order system and explain.	[4M]
	d)	Define absolute stability and relative stability.	[4M]
	e)	Define resonant frequency and cut off rate.	[4M]
	f)	What is meant by Observability?	[3M]

PART -B

2	a)	Write short notes on feedback control.	[4M]
	b)	Write the force equations of the linear translational system shown in the figure below. Draw the equivalent electrical network using force- voltage analogy, with the help of necessary mathematical equations.	[8M]



	c)	Draw the block diagram of a control system and explain its operation.	[4M]
3	a)	Obtain the transfer function C(s)/R(s) for the block diagram below using block diagram reduction technique.	[8M]



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b) Derive the transfer function of Synchro Pair. [8M]

4 a) Explain the effect of Proportional plus Derivative Control (PD) action on the performance of a second order system. [6M]

b) Determine the step, ramp and parabolic error constants of the following unity feedback control system whose open loop transfer function is given by [10M]

$$G(s) = \frac{1000}{(1+2s)(1+0.5s)}.$$

5 a) Using Routh-Hurwitz criterion, determine the stability of the closed loop system that has the following characteristic equation and also determine the number of roots that are in the right half s-plane and on the imaginary axis $3s^4 + 7s^3 + 2s^2 + s + 8 = 0$. [7M]

b) Find the angles of departure and arrival for all complex poles and zeros of the open loop transfer function of $G(s)H(s) = \frac{K(s^2 + s + 2)}{s(s^2 + 9)}, K > 0$. [9M]

6 a) Find resonant peak, resonant frequency and bandwidth of the unity feedback system whose open loop transfer function is $G(s) = \frac{1}{(s^2 + 6s + 5)}$. [8M]

b) The forward path transfer function of a unity feedback system is given by $G(s) = \frac{K}{(s+1)(s+2)}$. Using Bode diagram, determine the value of K so that the phase margin of the system is 45°. [8M]

7 a) Draw the electrical circuit diagram that represents the Lag-Lead Compensator and explain in detail. [8M]

b) Determine the state and output equations in vector matrix form for the system whose transfer function is given by $G(s) = \frac{(s+2)}{s(s^2 + 4s + 3)}$. [8M]

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Code No: RT31043 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
CONTROL SYSTEMS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
(Normal and semi & polar graph sheets are to be supplied)

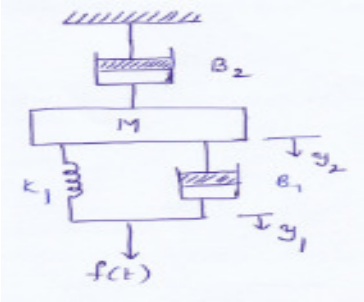
*****

PART –A

1 a) What is meant by closed loop control system? [3M]
b) What are the advantages of block diagram representation of a system? [4M]
c) Define Delay time and rise time. [4M]
d) Compare the stability of open loop and closed loop systems. [4M]
e) Define gain and phase margins. [4M]
f) What is meant by controllability? [3M]

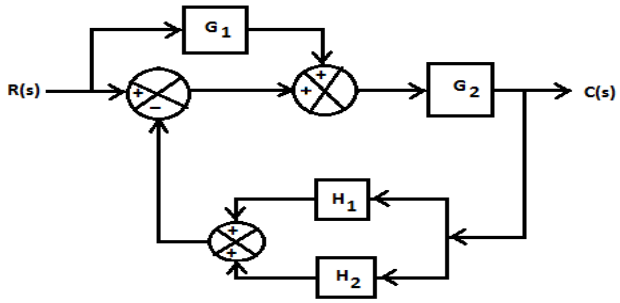
PART -B

2 a) Classify the control systems in detail. [4M]
b) Write the force equations of the linear translational system shown in the figure below. Draw the equivalent electrical network using force-voltage analogy, with the help of necessary mathematical equations. [8M]



c) Explain the effects of feedback on the system performance. [4M]

3 a) Using block diagram reduction techniques obtain the transfer function C(s)/R(s) for the block diagram below. [8M]



b) Derive the transfer function of AC servo motor. [8M]

||''|'''|''|'|'''||

4 a) Explain the effect of Proportional plus Integral Control (PI) action on the performance of a second order system. [6M]

b) Calculate the steady state errors due to a unit step input, a unit ramp input and a unit parabolic input for a unity feedback control system whose open loop transfer function is $G(s) = \frac{1}{(s^2 + 3s + 1)}$. [10M]

5 a) Using Routh-Hurwitz criterion, determine the stability of the closed loop system that has the following characteristic equation and also determine the number of roots that are in the right half s-plane and on the imaginary axis $s^3 + 2s^2 + s + 8 = 0$. [7M]

b) Find the angles of asymptotes and the intersect of the asymptotes of the root locus of the following equation when K varies from $-\infty$ *to* ∞ [9M]

$$s^3 + 5s^2 + s + K(s+1) = 0.$$

6 a) The forward path transfer function of a unity feedback system is given by $G(s) = \frac{K}{(s+3)^2}$. Using Nyquist Stability Criterion, determine the range of K for the closed loop system to be stable. [8M]

b) The forward path transfer function of a unity feedback system is given by [8M]

$$G(s) = \frac{K}{(s+1)^2}$$

Using Bode diagram, determine the value of K so that the gain margin of the system is 20 dB.

7 a) Draw the electrical circuit diagram that represents the Lead Compensator and explain in detail. [8M]

b) The state equation of a linear time invariant system is represented by [8M]

$$\frac{d\,x(t)}{dt} = A\,x(t) + Bu(t)$$

$A = \begin{bmatrix} 3 & 0 \\ 0 & -3 \end{bmatrix}, B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$. Find the state transition matrix and the Eigen values of A.

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Code No: RT31043 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015
CONTROL SYSTEMS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
(Normal and semi & polar graph sheets are to be supplied)

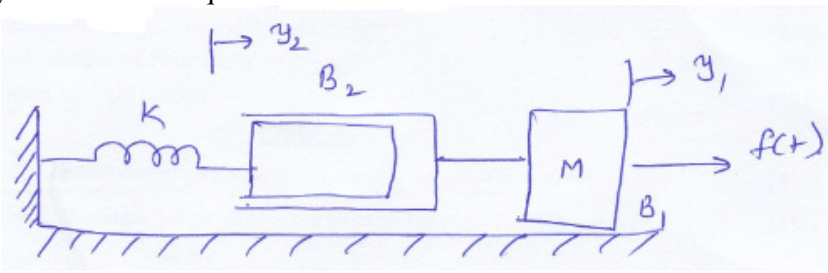
*****

PART –A

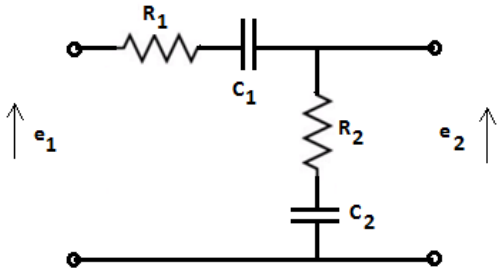
1	a)	What are the advantages of Mathematical Model?	[3M]
	b)	What are the advantages of transfer function representation of a system?	[4M]
	c)	Define maximum peak overshoot and settling time.	[4M]
	d)	Define qualitative stability and conditional stability.	[4M]
	e)	Explain the advantages of Polar plots.	[4M]
	f)	What does mean by state model?	[3M]

PART -B

2	a)	Compare the performances of closed loop and open loop control systems.	[4M]
	b)	Write the force equations of the linear translational system shown in the figure below. Draw the equivalent electrical network using force-voltage analogy, with the help of necessary mathematical equations.	[8M]



	c)	Derive the relationship that shows the effect of feedback on the overall gain of the system.	[4M]
3	a)	Obtain the transfer function $E_2(s)/E_1(s)$ for the electrical circuit below, by converting the circuit into a block diagram and then using block diagram reduction technique.	[8M]



	b)	Derive the transfer function of DC servo motor.	[8M]

||''|'''|''|'|'''||

4 a) Explain the effect of Proportional Control action on the performance of a second order system. [6M]

b) Calculate the steady state errors due to a unit step input, a unit ramp input and a unit parabolic input for a unity feedback control system whose open loop transfer function is $G(s) = \frac{1}{s^2(s+6)}$. [10M]

5 a) Using Routh-Hurwitz criterion, determine the stability of the closed loop system that has the following characteristic equation and also determine the number of roots that are in the right half s-plane and on the imaginary axis $s^3 + 3s^2 + 6s + 1 = 0$. [7M]

b) Find the angles of asymptotes and the intersect of the asymptotes of the root locus of the following equation when K varies from $-\infty$ *to* ∞ [9M]

$$(1+K)s^3 + (2+3K)s^2 + s(3-K) - 3K = 0.$$

6 a) The loop transfer function of a system is given by $G(s)\,H(s) = \frac{1}{s^3(s+2)}$. Draw the polar plot. [8M]

b) The loop transfer function of a system is given by $G(s)H(s) = \frac{25}{(s+2)^2}$. Using Bode diagram, find gain and phase margins of the system. [8M]

7 a) Draw the electrical circuit diagram that represents the Lag Compensator and explain in detail. [8M]

b) The state equation of a linear time invariant system is represented by [8M]

$\frac{dx(t)}{dt} = Ax(t) + Bu(t)$

$A = \begin{bmatrix} -3 & 0 \\ 0 & -3 \end{bmatrix}, B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$. Find the state transition matrix and the Eigen values of A

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Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November – 2015
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the data types available in VHDL?	[4M]
	b)	What is logic synthesis?	[3M]
	c)	What are the differences between PROM,PLA and PAL	[3M]
	d)	Explain the terms i) Noise margin ii) Transition time with respect to CMOS logic.	[4M]
	e)	Write a VHDL code for 1× 4 demultiplexer?	[4M]
	f)	Convert a D Flip-flop into T flip-flop	[4M]

PART –B

2	a)	Explain about data objects in VHDL.	[4M]
	b)	Explain the structure of various LOOP statements in VHDL with examples.	[8M]
	c)	Give the syntax and structure of a package in VHDL.	[4M]
3	a)	Define simulation? Explain about Gate-level simulation, Behavioral simulation and Functional simulation.	[8M]
	b)	Explain about inertial delay and Transport delay models in VHDL with examples.	[8M]
4	a)	Describe DRAM with an appropriate diagram and explain about its timings.	[8M]
	b)	Compare PROM, PAL and PLA.	[8M]
5	a)	Explain the CMOS circuit behavior with resistive load.	[8M]
	b)	Design a 2-input XOR and XNOR logic gates using CMOS logic.	[8M]
6	a)	Implement the 32 input to 5 output priority encoder using four 74LS148 & gates.	[8M]
	b)	Draw the logic diagram of IC 74180 parity generator checker and explain its operation with the help of a truth table.	[8M]
7	a)	Explain how a JK- flip-flop can be constructed using a T- flip-flop.	[8M]
	b)	Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style.	[8M]

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Code No: RT31044 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	What is HDL? Why do you need it?	[3M]
	b)	What is binding?Discuss the binding between library and components.	[4M]
	c)	Distinguish between SRAM and ROM.	[4M]
	d)	What are the advantages and disadvantages of CMOS technology?	[3M]
	e)	Write a VHDL program for 2x4 Decoder	[4M]
	f)	Convert a T flip-flop into a JK Flip-flop	[4M]

PART –B

2	a)	Write a VHDL program for n-bit ripple carry adder	[8M]
	b)	What are different data types available in VHDL? Explain.	[8M]
3	a)	What are the goals and objectives of Global routing and detailed routing?	[8M]
	b)	Explain the following: i) Timing constraints ii) Performance-driven synthesis iii) Circuit – level simulation.	[8M]
4	a)	With the help of timing waveforms, explain the read and write operations of static RAM.	[8M]
	b)	Design a BCD to Gray-code converter using PLA.	[8M]
5	a)	Design a 4 input CMOS OR-AND INVERT gate. Explain the circuit with the help of logic diagram and function table.	[8M]
	b)	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.	[8M]
6	a)	Write a VHDL code for 4-bit Look ahead carry generator.	[8M]
	b)	Design a 4×4 combinational multiplier and write the VHDL program in data flow model.	[8M]
7	a)	Design an Excess-3 decimal counter using 74 X 163 and explain the operation with the help of timing waveforms	[8M]
	b)	Give a VHDL code for a 4-bit upcounter with enable and clear inputs.	[8M]

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Code No: RT31044 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	What is Enumeration data type in VHDL? Give examples.	[3M]
	b)	Differentiate between Functions and Procedures in VHDL.	[4M]
	c)	List out the applications of ROM.	[3M]
	d)	Give the logic levels and noise margins of CMOS and TTL families.	[4M]
	e)	Write a VHDL program for 4x1 multiplexer	[4M]
	f)	Convert a T flip-flop into a D Flip-flop	[4M]

PART –B

2	a)	Discuss the binding? Discuss the binding between entity and components.	[8M]
	b)	Explain about signal assignment statements and Variable assignment statements with example.	[8M]
3	a)	What is the importance of time dimension in VHDL and explain its function.	[8M]
	b)	Discuss some of the important factors related to Synthesis.	[8M]
4	a)	Draw the block diagram of Synchronous RAM and explain its operation.	[8M]
	b)	Design an excess-3 to BCD code converter using PLA.	[8M]
5	a)	Design a 4 input CMOS AND-OR-INVERT gate. Explain the circuit with the help of logic diagram and function table.	[8M]
	b)	Explain about the steady state electrical CMOS behaviors for i) Resistive loads ii) Non ideal inputs	[8M]
6	a)	Design a priority encoder for 16 inputs using two 74×148 encoders.	[8M]
	b)	Write the VHDL program for fixed point to floating point conversion.	[8M]
7	a)	Design a 3 bit LFSR counter using 74×194.List out the sequence assuming that the initial state is 111.	[8M]
	b)	Draw the logic diagram of universal shift register and explain its operation.	[8M]

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Code No: RT31044 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Differentiate between VHDL and Verilog HDL.	[3M]
	b)	Write a test bench for two input XOR gate using VHDL.	[4M]
	c)	What are advantages of Programmable logic devices?	[3M]
	d)	List out the characteristics of ECL.	[4M]
	e)	Write a VHDL program for 4x2 encoder.	[4M]
	f)	Convert a JK Flip-flop into D Flip-flop.	[4M]

PART –B

2	a)	Explain about dataflow design elements of VHDL.	[8M]
	b)	What is binding? Discuss binding between entity and Architecture.	[8M]
3	a)	Write a VHDL program for comparing 8 bit unsigned integers.	[8M]
	b)	Discuss synthesis information from entity with examples.	[8M]
4	a)	Implement the following Boolean functions using a PLA $F1(A,B,C)= \Sigma\, m(0,1,3,5)$; $F2=(A,B,C)= \Sigma\, m(3,5,7)$.	[8M]
	b)	Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.	[8M]
5	a)	What is interfacing? Explain interfacing between low voltage TTL and low voltage CMOS logic.	[8M]
	b)	Design a transistor circuit of 2 input ECL NOR gate. Explain the operation with the help of function table.	[8M]
6	a)	Design a full adder using two half adders. Write VHDL program for the above implementation.	[8M]
	b)	Design a 16-bit comparator using 74×85IC's.	[8M]
7	a)	Design a 8 bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.	[8M]
	b)	Design a modulo – 100 counter using two 74 x 163 binary counters.	[8M]

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Code No: RT31042 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November - 2015
LINEAR IC APPLICATIONS
(Common to ECE, EIE and ECompE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Define differential amplifier and draw its block diagram.	[3M]
	b)	Define CMMR and give its ideal and practical values.	[4M]
	c)	Draw the non inverting op-amp circuit diagram and derive its output voltage.	[3M]
	d)	Draw the circuit diagram of all pass filter and write its output voltage equation.	[4M]
	e)	Draw the pin diagram of IC 555 and explain each pin.	[4M]
	f)	List out different Analog to digital convertors and justify which A/D convertor is best in terms of speed.	[4M]

PART -B

2	a)	Derive the Differential Amplifier- AC analysis of single input dual output Configuration in detail.	[8M]
	b)	Explain the concept of level translator in detail.	[8M]
3	a)	Explain the terms (i) slew rates (ii) CMRR (iii) PSRR (iv) drift and list out ideal and practical characteristics of above parameters.	[8M]
	b)	Explain the operation of Op-amp along with block diagram in detail.	[8M]
4	a)	Draw the circuit diagram of differentiator by using IC 741 and explain its operation.	[8M]
	b)	Explain the summer and difference amplifier using IC 741 and explain its operation.	[8M]
5	a)	Draw the block diagram of Sample & Hold amplifier and explain its operation in detail.	[8M]
	b)	Explain the operation of 2^{nd} order band reject filter along with circuit diagram.	[8M]
6	a)	Draw and Explain the principles and description of individual blocks of PLL in detail.	[8M]
	b)	Explain the terms frequency multiplication, frequency translation of PLL.	[8M]
7	a)	Draw the block diagram of inverted R-2R DAC and explain its operation in detail.	[8M]
	b)	List out the DAC and ADC Specifications and compare them in detail.	[8M]

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Code No: RT31042 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015
LINEAR IC APPLICATIONS
(Common to ECE, EIE and ECompE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Explain the purpose of level translator in differential amplifier.	[3M]
	b)	Draw the op-amp block diagram and explain the functions of each block.	[4M]
	c)	Draw the integrator circuit and derive its output equation.	[3M]
	d)	Define filters and draw the output characteristics of LPE and BPF filters.	[4M]
	e)	Draw the functional block diagram of IC 555 in detail.	[4M]
	f)	Define the terms Linearity and accuracy of A/D convertors.	[4M]

PART -B

2	a)	Derive the Differential Amplifier- AC analysis of Dual input single output Configuration in detail.	[8M]
	b)	Explain the Properties of other differential amplifier configuration in detail.	[8M]
3	a)	Explain the Frequency Compensation techniques of op-amp in detail.	[8M]
	b)	Draw the IC 741 op-amp pin diagram and explain the function of each pin in detail.	[8M]
4	a)	Draw the block diagram of log Amplifiers and explain its operation in detail.	[8M]
	b)	What are the limitations of log amplifier and how to overcome those limitations explain in detail.	[8M]
5	a)	Draw the block diagram of Four Quadrant multiplier and explain its operation in detail.	[8M]
	b)	Draw the 2^{nd} order band pass filter and draw its frequency response in detail.	[8M]
6	a)	Draw the astable applications of Schmitt Trigger and explain its operation in detail.	[8M]
	b)	Draw the circuit diagram of FSK demodulators and explain its operation in detail.	[8M]
7	a)	Draw the block diagram of dual slope ADC and explain its operation in detail.	[8M]
	b)	Draw the circuit diagram of weighted resistor DAC and explain its operation in detail.	[8M]

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Code No: RT31042 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
LINEAR IC APPLICATIONS
(Common to ECE, EIE and ECompE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Draw the differential amplifier block diagram and list out each block name.	[3M]
	b)	List out ideal and practical characteristics of Op-amp.	[4M]
	c)	Draw the precision rectifier circuit diagram.	[3M]
	d)	List out the applications of analog switches.	[4M]
	e)	Draw the block diagram of PLL and list out each block name.	[4M]
	f)	What are the basic DAC techniques?	[4M]

PART -B

2	a)	Derive the Differential Amplifier- DC analysis of Dual input Balanced output Configuration in detail.	[8M]
	b)	Explain the concept of Cascade Differential Amplifier Stages in detail.	[8M]
3	a)	Explain the IC 741 op-amp block diagram & its features in detail.	[8M]
	b)	List out the applications and Temperature ranges of IC 741 Op-amp.	[8M]
4	a)	Explain the operation of Square wave generators along with circuit diagram.	[8M]
	b)	Draw the block diagram of Non- Linear function generation and explain its operation.	[8M]
5	a)	Draw the block diagram of balanced modulator and explain its operation in detail.	[8M]
	b)	Draw the 2nd order band pass filter and explain its operation in detail.	[8M]
6	a)	Draw the block diagram of Astable operations using IC 555 and derive its time constant.	[8M]
	b)	Draw the circuit diagram of VCO 566 and explain its operation.	[8M]
7	a)	Draw the block diagram of successive approximation ADC and explain its operation in detail.	[8M]
	b)	Draw the circuit diagram of counter type ADC and explain its operation in detail.	[8M]

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Code No: RT31042 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015
LINEAR IC APPLICATIONS
(Common to ECE, EIE and ECompE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Explain different properties of differential amplifier.	[3M]
	b)	Explain different Package Types of op-amps.	[4M]
	c)	Draw the V to I and I to V convertor.	[3M]
	d)	List out the features of IC 1496 balanced modulator.	[4M]
	e)	What are the various applications of VCO 566?	[4M]
	f)	List out the DAC and ADC specifications in detail.	[4M]

PART -B

2	a)	Draw the dual input and dual output differential amplifier and derive its ac characteristics in detail.	[8M]
	b)	Draw the circuit diagram of level translator and explain its operation in detail.	[8M]
3	a)	Explain different frequency compensation techniques of op-amp in detail.	[8M]
	b)	Explain the terms (i) Input & Out put Off set voltages & currents, (ii) slew rates, (iii) CMRR and (iv) PSRR.	[8M]
4	a)	Draw the Instrumentation amplifier and explain its operation in detail.	[8M]
	b)	Draw the Anti log Amplifiers circuit diagram and derive its output voltage in detail.	[8M]
5	a)	Draw the circuit diagram of Sample & Hold amplifier and explain its operation in detail.	[8M]
	b)	Draw the circuit diagram of All pass filters and derive its output response.	[8M]
6	a)	Draw the circuit diagram of Monostable multivibrator by using IC 555 timer and explain its operation.	[8M]
	b)	Draw the block diagram of PLL and explain the operation of individual blocks in detail.	[8M]
7	a)	Draw the block diagram of parallel Comparator type ADC and explain the operation of it.	[8M]
	b)	Draw the block diagram of R-2R ladder DAC and explain its operation.	[8M]

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Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November- 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Define storage time and transition time of a diode.	[3M]
	b)	What are the advantages and disadvantages of a direct coupled binary?	[4M]
	c)	What do you mean by phase jitter?	[3M]
	d)	State and prove clamping circuit theorem.	[4M]
	e)	What do you mean by Schotty TTL? Why is it faster than standard TTL?	[4M]
	f)	What does the display of a sampling scope consists of?	[4M]

PART -B

2	a)	Prove that a low pass circuit acts as an integrator. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input.	[8M]
	b)	Explain RLC ringing circuit with a neat sketch.	[8M]
3	a)	Define i) Rise time ii) Fall time iii) Delay time iv) Storage time Explain the factors which contribute to the delay time of transistor.	[8M]
	b)	Draw the circuit of CMOS NOR gate and explain its operation. Mention the advantages of CMOS over the other digital logic families.	[8M]
4	a)	Describe the sequence of events in an n-p-n transistor to change from cutoff to saturation and vice versa. How does temperature affect the saturation junction of a transistor?	[8M]
	b)	Draw and explain the circuit diagram of integrated positive TTL AND & OR gates.	[8M]
5	a)	Explain the operation of a Monostable multivibrator and derive for the pulse width with necessary waveforms & circuirts.	[8M]
	b)	Design a collector coupled astable multivibrator using NPN silicon transistors with h_{fe}=40, r_{bb}=200Ω supploied with Vcc=10V and circuit component values are Rc=1.2KΩ and C=270 pF.	[8M]
6	a)	Explain the working of a transistor Bootstrap sweep circuit and derive expression for the slope sweep error.	[8M]
	b)	Why the time base generators are called sweep circuits? Give most important applications of time –base generators.	[8M]
7	a)	Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate.	[8M]
	b)	Draw and explain the waveforms of a frequency division by an Astable multivibrator.	[8M]

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Code No: RT31041 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

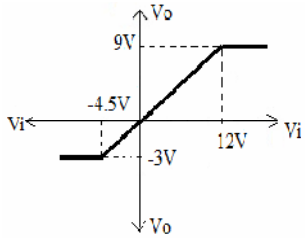
*****

PART –A

1	a)	What are the reasons for existence of rise time and fall time?	[4M]
	b)	Why a monostable multivibrator is also called a delay circuit? Explain.	[3M]
	c)	What do you mean by synchronization on a one-to-one basis and that with frequency division?	[4M]
	d)	Which logic gates are suitable for wired OR operations and why?	[3M]
	e)	What do you mean by pedestal? What are the advantages of diode sampling gates?	[4M]
	f)	What is hysteresis how it can be eliminated in a Schmitt trigger?	[4M]

PART -B

2	a)	Draw the output waveform of an RC high-pass circuit with a square wave input under different time constants. Derive the expression for percentage of tilt.	[8M]
	b)	Draw a Schmitt Trigger using transistors and derive for UTP & LTP.	[8M]
3	a)	Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics	[8M]
	b)	State and prove clamping circuit theorem.	[4M]
	c)	The ideal transfer characteristic of particular clipper circuit is shown in Figure.2. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if Vi = 15 Sin ωt.	[4M]



4	a)	Explain with the help of suitable waveforms the switching times of a diode switch. Derive the expression for reverse recovery time.	[8M]
	b)	Draw and explain the circuit diagram of integrated positive RTL NOR gate.	[6M]
	c)	Explain the reason for delay transition in a transistor as a switching element.	[2M]
5	a)	Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with $h_{FE(min)}$ =20. In stable state, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the $I_{B(min)}$ value. Assume VCC = 8V, IC(sat) =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R1, C and V_{BB} .	[8M]

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b) Draw the circuit diagram of an astable multivibrator and obtain all the steady state voltages and currents. Show how it acts as a voltage to frequency converter. [8M]

6 a) What are the different methods of generating time-base waveforms? Explain about each briefly. [8M]

b) Explain the working of Transistor Miller sweep circuit. What are its advantages over Bootstrap sweep circuits? [8M]

7 a) With the help of a neat circuit diagram and waveforms, explain the method to achieve frequency synchronization using pulse train as sync signals. [8M]

b) Explain the function of a sampling gate used in Sampling Scopes also explain how sampling gate is used in chopping amplifiers. [8M]

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Code No: RT31041 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

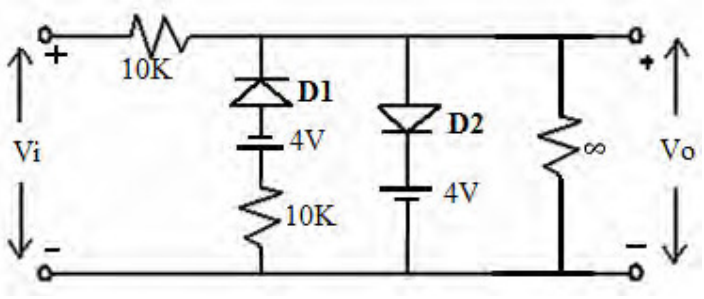
Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
*****

PART –A

1	a)	What is direct coupled binary? Give its advantages and disadvantages.	[4M]
	b)	What do you mean by blocked condition in astable multivibrator?	[3M]
	c)	How is the deviation from linearity expressed?	[3M]
	d)	What do you mean by synchronization? When do we say two waveform generators are synchronized?	[4M]
	e)	What are the advantages of MOS families over bipolar families?	[4M]
	f)	What are the advantages and disadvantages of unidirectional diode gates?	[4M]

PART -B

2	a)	Derive an expression for the output of low pass RC circuit excited by a step input. Draw the output for different time constants.	[8M]
	b)	What is an attenuator? How can an uncompensated attenuator be modified as a compensated attenuator. Give the comparison between perfect compensation, under compensation and over compensation.	[8M]
3	a)	Explain the working of a two-level diode clipper with the help of circuit diagram, waveform and transfer characteristics.	[6M]
	b)	Determine the output waveform for the biased clipping circuit for the square wave input.	[6M]
	c)	A voltage signal of (10 Sinωt) is applied to the circuit with ideal diodes shown in figure below. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation	[4M]



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4 a) Briefly discuss the influence of breakdown voltages on the choice of supply voltage in a transistor switch. [4M]

b) Explain the characteristics and implementation of the following digital logic family i) CMOS, ii) ECL [8M]

c) Classify the basic families that belong to the bipolar families and to the MOS families. [4M]

5 a) b) Design a Schmitt trigger circuit using npn silicon transistors with V_{BE} = 0.7V, $V_{CE}(sat)$ = 0.2V, $h_{fe}(min)$ = 60 and $I_C(ON)$ = 3mA to meet the following specifications: V_{CC} =12V, upper threshold voltage, V_{UT} = 4V, lower threshold voltage, V_{LT} =2V. [8M]

b) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary. [8M]

6 a) Define and derive the terms slope error, displacement error and transmission error. [8M]

b) Explain the basic principles of Miller and Bootstrap time-base generators. Give the comparison of both the generation methods. [8M]

7 a) What is synchronization? Why it is necessary in waveform generators? Explain the synchronization of a sweep circuit with symmetrical signals. [8M]

b) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram. [8M]

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Code No: RT31041 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
*****

PART –A

1	a)	Which signal can preserve its wave shape when transmitted through a linear network and explain how it can.	[4M]
	b)	Show the relationship between the percentage of tilt and cutoff frequency for a high pass RC circuit.	[3M]
	c)	What are the applications of time base generators?	[3M]
	d)	What is non-saturated binary? What are its drawbacks?	[4M]
	e)	What are the merits and demerits of TTL?	[4M]
	f)	Why sampling gates called linear gates and how do they differ from logic gates?	[4M]

PART -B

2	a)	An RC low-pass filter is fed with a symmetrical square wave. The peak-to-peak amplitude of the input waveform is 10 V and its average value is zero. It is given that RC=*T/2* where *T* is the period of the square wave. Determine the peak-to-peak amplitude of the output waveform.	[8M]
	b)	Draw the response of an RC high pass circuit when applied with exponential input. Explain the response for different time constants.	[8M]
3	a)	Draw the circuit diagram and explain the working of transistor clippers.	[6M]
	b)	Draw the basic circuit diagram of negative peak clamper circuit and explain its operation	[7M]
	c)	Give some applications of clipping & Clamping circuits.	[3M]
4	a)	Describe how a transistor functions as a switch in the CE configuration in ON state and in OFF state. How does the temperature affect the saturation junction voltages of a transistor?	[8M]
	b)	Classify the basic families that belong to the bipolar families and to the MOS families.	[4M]
	c)	What is the major difference between TTL and ECL? Why does the propagation delay occur in logic circuits?	[4M]

5 a) A self-biased binary uses n-p-n transistors have maximum values of V_{CE}(sat)=0.4V and V_{BE}(sat) = 0.8V and V_{BE} (cutoff) = 0V. The circuit parameters are V_{CC} = 15V, RC = 1KΩ, R1 = 6KΩ, R2 = 15KΩ and RE = 500Ω. i) Find the stable-state currents and voltages. ii) Find the minimum value of hFE required for BJT to provide the above stable state values. iii) Also determine I_{CBO}(max) to which I_{CBO} raises as temperature rises where neither BJT is off. [8M]

b) Explain various methods to improve the resolution of a binary. [4M]

c) Draw the circuit of a Schmitt trigger and give some of its applications. [4M]

6 a) Explain the basic principle of a bootstrap sweep generator. Draw the circuit and explain its operation. Derive the expression for its slope error. [8M]

b) How is deviation of linearity expressed? What do you mean by sweep time and restoration time? [8M]

7 a) What is meant by synchronization with frequency division? Explain, with suitable waveforms, the procedure to obtain 3:1 and 5:1 synchronization. [8M]

b) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. [8M]

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