Diet

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NAAC Accredited Institute and Inclusion under Section 2(f) of UGC Act
An ISO 9001:2008; ISO 14001:2004 & OHSAS 18001:2007 Certified Institution

NH-16, Anakapalle – 531002, Visakhapatnam, A.P.

Mobile: +91 9963981111, Website: www.diet.edu.in, E-mail: info@diet.edu.in

Academic year: 2020-21

Anakapalle, Dt: 06-08-2020

From,
Mr. KJogi Naidu,
HOD - ECE,
Dadi Institute of Engineering & Technology.

(Through Proper Channel)

To.

The Principal,

Dadi Institute of Engineering & Technology.

Sir,

Sub: Permission for Conduction of GATE Classes for IV-I B. Tech ECE Students- Reg

With due respect, here by stating that, I, on behalf of ECE Department request you for conduction of GATE Classes for our ECE IV-I B.Tech students who are under eligible criteria and are also interested. The GATE Class work schedule is planned for 3 hours on every Saturday without hindering the regular classwork, the time table schedule will be shared a week prior to commencement of IV-I Regular class work.

We, therefore, hope that you would be kind enough to permit us to conduct the GATE Classes. Kindly grant us the permission. Awaiting anxiously for your reply.

Thanking you Sir,

Yours Sincerely,

DIFT

Cleatronics & Con-surviviors to Dadi Institute (Con-surviviors)

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CIRCULAR

DATE:13/08/2020

This is to inform all the IV-I B.Tech ECE Students that the Department of ECE is Conducting GATE Classes for interested and eligible students on every Saturday from the day of beginning of your IV-I Class work. So students of IV-I B.Tech ECE are instructed to kindly make the best use of this opportunity. The subject schedule and time table will be shared accordingly.

HAPPY LEARNING & ALL THE VERY BEST!!

Venue: LH-29

Head of the Department Sectionics & Communication Eng Oads Institute of Engly, & Tech

Anakanabe 531007

PRINCIPAL

PRINCIPAL
Dadi Institute of
Engineering & Technologs
ANAKAPAILE - 531 002



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NAAC Accredited Institute

An ISO 9001:2008, 14001:2004 & OHSAS 18001:2007 Certified Institute

Dept. Name -ECE NH-5, Anakapalle, Visakhapatnam-531002, Andhra Pradesh

w.e.f: 22-08-2020 Course / Year / Sem -B.Tech/ IV/ I Section: B Academic Year - 2020-21 Class Teacher - Mr.M.Suneel Kumar Total Strength- 47 Lecture Hall -

Mad	Mrs. Di Markai A. C		Lab	Digital Signal Processing Lab	Digital	DSP	2
mesh	Mr.KSNV Someshwara	-	o l oh	Microwave Engineering Lab	Micro	MWE	1
		ORY	LABORATORY				
enneti	MIS.Laxmi Yeni		35	GATE Classes		GATE	-
ekhar	MILA Soma Sek		stems	Embedded Systems		ES	0
1	Mrs.Karchana		Electronic Switching Systems	Electronic S		ESS	5
8	Mrs.G Sujatha		munications	Optical Communications		00	4
	Mr.S.Balaji		atworks and	Computer Networks	1	CN	Ļ
lavi	Mrs. K Madhav		Digital Image Processing	Digital Imag		DIP	2
ē	Faculty name		ns Jest tall	Radar Systems		RS	-
			Subject Name		le	Sub.Code	S.No
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Mobile: +91 9963981111, Website: www.diet.edu.in, E-mail: info@diet.edu.in

DEPARTMENT OF ECE GATE HANDLING FACULTY- 2020-21

S.NO	SUBJECT	FACULTY
i	Network Analysis	R.Suneel Kumar
2	Digital Electronics	D.Ravi Nayak
3	Signal and Systems	k.Jagan Mohan panigrahi
4	Control Systems	M.Kishore Kumar
5	Communication Systems	K.Someswara Rao
6	Analog Electronics	K.Jogi Naidu
7	Electronic Devices and Circuits	P.Poorna Priya
8	Electromagnetic Theory	M.Kasiyammal

Maidu

Proad of the Department
Electronics & Communication L
Dads Institute of Engl & Tech
Anaxapalle 531 002

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Dadi Institute of
Engineering & Technolog
ANAKAPALLE - 531 962

Dadi Institute of Engineering & Technology, Anakapalle SYLLABUS COVERAGE REPORT



SI. No.	Date	Time	No.of Periods engaged	Topic Covered Network Theory	REMARKS
1.	22 5 21		3	Baric Concepts of network	
	dest see			Network theory, Francient	
				-Analysis.	
2.	29 8 21		A	Two port networks, sinusoida	
				state analysis, Phasor Locus	2-2-3
				diagram à complèx ponu	
3.	12/9/21	- 1	3	Resonance, Network functions	
	10.000			* filter, Graph theory	
				Digital Electronics	
4.	19/9/-1		3	Boolean Algebra, Number	
-				systems, Logic gates.	
5	20/9/31		3	K-Maps, combinational Logic	
				Design, sequential circuits,	
	- No. (240)			ADC, DAC.	
6	03 10 21		3	Microprocessors, Machine	
\dashv		- 25	_	instructions & addressing made	u
				Instructions pipelining	0100
				signal a systems	100
7.	10/10/24		3	classifications & types of	
-				Signals, Fourier Represental	To.
4				of periodic & Aperiodic	Corca
-				Signals	
8	14/10/14		3 .	Fourier transform DTFT,	
-				DFT, FTI of standard	
- 1	-	- 22		signals.	
9.	81/10/21		3	Laplace transform, & transform	
-		-		all standard commely	
-				Postfal Fraction method,	3 30 3
				33.1.504)	
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Dadi Institute of Engineering & Technology, Anakapalle SYLLABUS COVERAGE REPORT



_		-	1	
SI. No.	Date	Timo	No of Feriods engaged	Topic Covered REMARK
10.	=1 11 21		3	Block diagrams a ingred
	wilders in the			flow graph, time
	cara br		8	Roof locus, stability
il.t	14/11/51			Catteria, Nyquist (lability
			100	Conterior, Polar plots,
12	भागम		3_	Bode plots frequesponse of
				controllers compensators.
			1	
				Communication system
_			-	Note in -Analog Communication
13.	म्ह्रीर्गान		3	Random Variables & Random
				process.
ių.	05/12/24		3	Noise in digital communication
-			-	Information theory & coding
				Analog Electronics
			-	2000
15.	12/12/24		3	
_				Operation Small signal
		-		analysis
16,	19/12/21		3	Freq. response of BIT analysis
		-		MOSFET biaring, operational
				Amplifiers, Feedback
	26/12/21		.3	Active filters, concert micros,
	1-1-1			a differential amplifiers
=				Oscillator Cincina
-				Hartley, colpitts.
_		-		**

Dadi Institute of Engineering & Technology, Anakapalle SYLLABUS COVERAGE REPORT

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W	IG	L

SI. No.	Date	Time	No of Periods engaged	Topic Covered	REMARKS
				Electronic Ornice + circuit	
18	02(01/22		3	Semiconductor Physics Introduction, PN Tunction	
				diode, Introduction to	
14-	19 01 22		3	JEET, MOSFET, Special purpose diodes.	
				Electromagnetic theory	
20.	23/01/22		a	Fred amentals, Transmime	m
		t.i.		Posterna a Padration Posterna Metallic Navegni	16 Organ
	-				
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NH-16, Anakapalle – 531002, Visakhapatnam, A.P.

Mobile: +91 9963981111, Website: www.diet.edu.in, E-mail:

info@diet.edu.in

Department of ECE

FEEDBACK FORM ON

GATE 2020-21

1. Di	d the GATE Schedule attained its objectives Yes
	No
2. GA	ATE Training was relevant to my needs
	Strongly agree
	Agree
	Neutral
	Disagree
	Strongly disagree
3. I	nstructions were clear and understandable
	Strongly agree
	Agree
	Neutral
	Disagree
	Strongly disagree
4. Co	ontent was well organised
	Strongly agree
	Agree
	Neutral

5. Was the Duration of the training sufficient.
□ Yes
□ No
6.Resource persons were effective.
□ Strongly agree
□ Agree
□ Neutral
□ Disagree
□ Strongly disagree
7. Queries were encouraged
□ Strongly agree
□ Agree
□ Neutral
□ Disagree
☐ Strongly disagree
8. Any additional remarks
9. Overall how would you rate this schedule.
□ Excellent
□ Very good
\Box Good
□ Fair
□ Poor

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Department of ECE

GATE Syllabus for ECE – General Aptitude

- Verbal Ability:
 - Instructions,
 - English grammar,
 - Verbal deduction,
 - Word groups
 - Sentence completion,
 - Critical reasoning
 - Verbal analogies.
 - Numerical Ability
 - Numerical reasoning
 - Numerical computation,
 - Data interpretation, and
 - Numerical estimation.

GATE ECE Syllabus for Engineering Mathematics

Vector Analysis:Gradient, Vectors in plane and space, Divergence and curl, Vector operations, Green's, Gauss's, and Stoke's theorems. Linear Algebra: Matrix algebra, Vector space, Eigen-values & eigen vectors, Basis, Rank, solution of linear equations: Existence, and Uniqueness. Linear dependence and independence,

Probability and Statistics:

- Mean, median, mode and standard deviation,
- Combinatorial probability,

- Joint and conditional probability,
- probability distribution functions:
 - Binomial,
 - Exponential,
 - Poisson, and
 - Normal.

Calculus:

- Maxima and minima,
- Mean value theorems,
- Taylor series,
- Theorems of integral calculus,
- Multiple integrals,
- Evaluation of definite and improper integrals,
- Surface and volume integrals,
- Partial derivatives,
- Line.

Complex Analysis:

- Cauchy's integral formula,
- Analytic functions,
- Residue theorem,
- Cauchy's integral theorem,
- Taylor's and Laurent's series.

Differential Equations:

- Particular integral & Complementary function,
- First order equations (nonlinear and linear),
- Initial & boundary value problems,
- Higher order linear differential equations,
- Partial differential equations,
- Cauchy's & Euler's equations,
- Variable separable method,
- Methods of solution using the variation of parameters.

Numerical Methods:

- Single & Multi-step methods for differential equations,
- Convergence criteria,
- Solution of nonlinear equations.

GAE Syllabus for ECE – Networks, Signals and Systems

- Network solution methods:
 - Solution of network equations using Laplace transform,

- Nodal and mesh analysis,
- State equations for networks,
- Time domain analysis of simple linear circuits,
- Network theorems:
 - Superposition,
 - Maximum power transfer
 - Thevenin and Norton's.
- Frequency domain analysis of RLC circuits,
- Wye-Delta transformation,
- Linear 2-port network parameters:
 - Driving point and
 - Transfer functions.
- Steady state sinusoidal analysis using phasors.

Continuous-time signals:

• Discrete-time signals:Z-transform,Discrete-time Fourier transform (DTFT),Interpolation of discrete-time signals,FFT,DFT.

Fourier series and Fourier transform representations, LTI systems:

- Poles and zeros,
- Definition and properties,
- Digital filter design techniques,
- Causality,
- Parallel and cascade structure,
- Stability,
- Phase delay,
- Impulse response,
- Frequency response,.

Syllabus of GATE ECE 2020 – Electronic Devices

- BJT,
- Energy bands in intrinsic & extrinsic silicon,
- Integrated circuit fabrication process:
 - Ion implantation,
 - Oxidation,
 - Photolithography & twin-tub CMOS process,
 - Diffusion.Carrier transport:

- Resistivity,
- Diffusion current,
- · Mobility, and
- Drift current.

MOS capacitor,

Generation and recombination of carriers,

Photo diode and Solar cell,

Poisson and continuity equations,

MOSFET,

P-N junction,

LED

Zener diode.

GATE 2020 Syllabus for ECE – Analog Circuits

- Active filters,
- Small signal equivalent circuits of diodes,
- Power supplies:
 - Ripple removal, and
 - Regulation.

BJTs and MOSFETs,

Sinusoidal oscillators:

- Criterion for oscillation,
- Single-transistor & op-amp configurations.
- Simple diode circuits:
 - Clamping,
 - Clipping, and
 - Rectifiers

Voltage reference circuits,

Single-stage BJT and MOSFET amplifiers:

- Biasing,
- Mid-frequency small signal analysis,
- Bias stability, and
- Frequency response.

Function generators,

BJT and MOSFET amplifiers:

- Multi-stage,
- Differential,

- Feedback,
- Power & operational.

Wave-shaping circuits and 555 timers, Simple op-amp circuits.

GATE 2020 ECE Syllabus – Digital Circuits

- Data converters:
 - ADCs and DACs,
 - Sample & hold circuits.

Number systems,

8-bit microprocessor (8085):

- Programming,
- Architecture,
- Memory and I/O interfacing.

Combinatorial circuits:

- Code converters,
- Boolean algebra,
- Decoders and PLAs,
- Arithmetic circuits,
- Minimization of functions using Karnaugh map & Boolean identities,
- Multiplexers,
- Logic gates & their static CMOS implementations.

Semiconductor memories:

- ROM.
- DRAM,
- SRAM.

Sequential circuits:

- Shift-registers,
- Latches & flip-flops,
- Finite state machines,
- Counters.

GATE Exam Syllabus ECE 2020 - Control Systems

- Transient & steady-state analysis of LTI systems,
- Basic control system components,
- Lag, lead & lag-lead compensation,

- Frequency response,
- Feedback principle,
- Bode and root-locus plots,
- State variable model,
- Transfer function,
- Solution of state equation of LTI systems,
- Block diagram representation,
- Routh-Hurwitz and Nyquist stability criteria,
- Signal flow graph.

GATE Syllabus for ECE 2020 – Communication

- Fundamentals of error correction,
- Random processes:
 - Autocorrelation & power spectral density,
 - Filtering of random signals through LTI systems,
 - Properties of white noise.

Basics of

- TDMA,
- CDM
- FDMA.

Analog communications:

- Superheterodyne receivers,
- Amplitude modulation & demodulation,
- Circuits for analog communications,
- Angle modulation & demodulation,
- Spectra of AM and FM.

Hamming codes,

Information theory:

- Entropy
- Channel capacity theorem,
- Mutual information.

Inter-symbol interference and its mitigation,

Digital communications:

- Phase and frequency shift keying (PSK, ASK, FSK),
- PCM,
- SNR and BER for digital modulation,
- DPCM,

- QAM, MAP and ML decoding,
- Digital modulation schemes,
- Calculation of bandwidth,
- Amplitude,
- Matched filter receiver.
- Timing & frequency synchronization.

GATE 2020 Syllabus ECE – Electromagnetics

- Waveguides:
 - Cut-off frequencies,
 - Modes,
 - Dispersion relations,
 - Boundary conditions.

Electrostatics,

Light propagation in optical fibers,

Maxwell's equations:

- Wave equation,
- Differential & integral forms and their interpretation,
- Poynting vector,
- Boundary conditions.

Antennas:

- Return loss,
- Antenna types,
- Fain and directivity,
- Antenna arrays,
- Radiation pattern.

Plane waves and properties:

- propagation through various media,
- Reflection and refraction,
- Phase and group velocity,
- Skin depth,
- Polarization.

Basics of radar,

Transmission lines:

- Impedance transformation,
- Equations.

- S-parameters,Characteristic impedance,
- Smith chart,
- Impedance matching.

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DETAILED REPORT ON CONDUCTION OF GATE CLASSES(2020-21)

GATE exam has gained a lot of Importance as students who qualify GATE are eligible for direct recruitment in PSUs like BPCL, ONGC, BARC, NTPC, NPCIL, GAIL, BHEL, DRDO, IOCL, NALCO, CtC.HOD ECE visited all the final year ECE classes and highlighted the importance of GATE exam for PSUs as well as higher studies. This improved the enrolment ratio from around 45% in year 2018-19 to around 72% in consecutive years. GATE (2020-21) Classes have been handled for IV ECE Students from 22/08/2020 for 2017 admitted batch students and 8 Subjects have been handled by different faculty as stated In the list and they covered the topics from previous gate papers. Training of 60 hrs along with 4 to 5 mock test is scheduled for students appearing GATE 2020.The students participating in GATE Training were also provided with the entire set of notes consisting of Important topics and useful for further preparation.

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Mobile: +91 9963981111, Website: www.diet.edu.in, E-mail: info@diet.edu.in

Academicyear: 2017-18

From.

R.V.S Lakshmi Kumari

HOD-EEE.

Dadi InstituteofEngineering&Technology.

Anakapalle, Dt:09-08-2017

(ThroughProperChannel)

To.

ThePrincipal,

Dadi Institute of Engineering & Technology.

Sir.

Sub:Permission forConductionofGATE Classesfor IV-IB. TechEEE Students-Reg.

With due respect I here by stating that ,I, on behalf of EEE Department request you for conduction of GATE Classes for our EEE IV-I B.Tech students who are under eligible criteria and are also interested .The GATE Class work schedule is planned for 3 hours on every week without hindering the regular class work,the time table schedule will be shared a week prior to commencement of IV-I Regular class work.

We, therefore, hope that you would be kind enough to permit us to conduct the GATE Classes. Kindly grant us the permission. Awaiting anxiously for your reply.

ThankingyouSir,

ours Sincerely, HOD-EEE, DIET

Head of the Department Electrical & Electronics Enda Dadi Institute of Engg. & Tec-

Anakapalle - 531 002

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Mobile: +91 9963981111, Website: www.diet.edu.in, E-mail: info@diet.edu.in

CIRCULAR

DATE:17/08/2017

All the students of IV year B.Tech students here by informed that the GATE notification had been released on 09TH August 2017. The exam will be in February 2018 through online mode. The last date for applying GATE exam is 17th Nov 2017. The EEE department is going conduct gate classes from 22nd November 2017. So students of IV-I B.Tech EEE are instructed to kindlymakethebestuse of this opportunity. The subjects chedule and time table will be shared accordingly.

HAPPYLEARNING&ALLTHEVERY BEST!!

Venue:LH-37

Head of the Department

Electrical & Electronics E Dadi Institute of Engg. F

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	9:00 09:50	09:50- 10:40	BR	10:50 - 11:40	11:40 12:30		1:00 - 1:50	1:50 - 2:40	2:40 - 3:30	3:30-4:15
MON	HVAC/D C	EDS		PSOC	HVA C/DC		Project	PSOC	RES	GATE
TUE	HVAC/D C	(Sin	mulatio	on /MPM(C)	_	PSOC	RES	INST	GATE
WED	RES	(I	PSLAB	/MPMC)		LUNCH	EDS	RES	INST	GATE
THU	PSOC	EDS		HVAC /DC	EDS	H	INST	RES	INST	SPORTS
FRI	INST	HVAC/ DC	EAF	RES	INST		GATE	PSOC	EDS	LIB

EDS

S.No	Sub Code	Subject Name	No of Perio ds	Name of the faculty
		THEORY		N, and the second secon
1	RES	Renewable energy sources	6	Ms.GPrasoona
2	HVAC &DC	High voltage AC/DC	7	Mr.DVNAnanth
3	PSOC	Power System operation &controll	6	Mr. M Raja Rao
4	INS	Instrementation	6	Mrs.AL Durga
5	EDS	Electrical Distribution systems	6	Mr.MRajendra Prasad
6		Gate classes	3	

HVAC

Total theory hours - 31 Department Total Lab hours - Head of the Department Total Lab hours - 1

HVAC

PSOC

Sports - 1

RES.

(Reme

dial)

(Simulation /PS LAB)

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DEPARTMENTOFEEE GATEHANDLINGFACULTY-2017-18

S.NO.	SUBJECT	FACULTY
1	NetworkAnalysis	M.Rajarao
2	DigitalElectronics	G.Jagadeesh
3	Signal and Systems	B.N.Srinivasarao
4	ControlSystems	K.vijayakumar
5	Power systems	A.Lakshmidurga
6	Electrical machines	CH.Nookesh
7	Electrical measurements	CH.Ravikumar
8	Power electronics	J.Dileepkumar

Head of the Department Electrical & Electronics Engg. Institute of Engg. & Tech. Andranalle - 1531 00

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Dadi Institute of Engineering & Technology

ANAKAPALLE - 531 002

Dadi Institute of Engineering & Technology, Anakapalle SYLLABUS COVERAGE REPORT

	606			
SI. No.	Date	No.of Periods engaged	Topic Covered	REMARKS
(D)	27 Julia	neuro pri propriemente con estra de como solo por estable de la como de la co	Basics of PC Machines	
0	30/11/17	angeneralizateur reneralizateur interesteur. O B republikateur interesteur interesteur.	Introduction to Electrical Circuit	1
3	1/12/17	- new properties of the second	Interoduction to Measurements	
9	4/12/17	0)	-types of M.I Parls of DCMachine, Working of DCMachine	
3	8/12/17	0)	PSA-Single line diagram	
6	10/12/17	01	Basic fundamentals circuits	
<u>(1)</u>	15/12/17	01	Deflecting toeque in Valuous. types of instluments Aimature reaction.	
8	17/12/17	0	Alimature reaction.	
9	21/12/17	01	Block diagram seduction	
(6)	22/12/13	01	Belies and faciallel Connection	
(ii)	23/12/17	0/	Shunt Pelies multiplieus	
0	29/12/17	01	Types of windings	
(B)	30/12/17	0/	Peroblems on PU system.	
<u> </u>	4/01/18	0/	Ac circuit franameters (R,L,C	
(B)	8/01/18	0/	chaeacteristics of DC generate	du:
(b)	11/01/18	01	Gate Papers solving.	9
	12/1/18	0	Gate Papels Solving.	

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Dadi Institute of Engineering & Technology, Anakapalle SYLLABUS COVERAGE REPORT

31.	Date	No.of Periods engaged	Topic Covered	REMARKS
1	19/1/17	01	Parallel operation condition for DC generato Paper Solving/electrical	
1	20/1/17	01	Papel solving/electrical	Ct
	28 1/17	0)	Paper Solving Etts.	
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DepartmentofEEE

FEEDBACK FORM ON **GATE 2017-18**

1.	DidtheGATESchedule attaineditsobjectives
	Yes
	No
2.	GATETrainingwasrelevantto myneeds
	Stronglyagree
	Agree
	Neutral
	Disagree
	Stronglydisagree
3.	Instructionswereclearandunderstandable
	Stronglyagree
	Agree
	Neutral
	Disagree
	Stronglydisagree
4. (Contentwaswellorganized
	Stronglyagree
1	Agree
	Neutral
J	Disagree
	그리 맛이 그는 프로젝트를 하는 것이 되었다. 이번 모르는 그 그리고 있는 것은 그리고 말했다. 그리고 있다.

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5. W	astheDurationof thetrainingsufficient.			
	Yes			
	No			
6.Re	esourcepersonswereeffective.			
L	Stronglyagree			
П	Agree			
	Neutral			
	Disagree			
	Stronglydisagree			
7. Q	ucricswercencouraged			
	Stronglyagree			
	Agree			
	Neutral			
	Disagree			
	Stronglydisagree			
	[발생] [발표] [발표] [발표] [발표]			
8. A	nyadditionalremarks			
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	verallhowwouldyouratethisschedule?			
	Excellent			
	Verygood			
	Good			
	Fair			
	Poor			

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DepartmentofEEE

GATE Syllabus for EEE-General Aptitude

- · Verbal Ability:
 - · Instructions.
 - · English grammar,
 - · Verbal deduction,
 - Word groups
 - Sentence completion,
 - Critical reasoning
 - Verbal analogies.
 - · Numerical Ability
 - · Numerical reasoning
 - · Numerical computation,
 - Data interpretation ,and
 - Numerical estimation.

GATE EEE Syllabus for Engineering Mathematics

Vector Analysis: Gradient, Vectors in plane and space, Divergence and curl, Vector operations, Green's, Gauss's, and Stoke's theorems

LinearAlgebra:Matrixalgebra,Vectorspace,Eigenvalues&eigenvectors,Basis,Rank, solution of linear equations: Existence, and Uniqueness .Linear dependence and independence,

Probability and Statistics:

- Mean, median, mode and standard deviation,
- Combinatorial probability,
- Joint and conditional probability,
- Probability distribution functions:
 - Binomial,

- Poisson, and
- · Normal.

Calculus:

- · Maximaandminima,
- · Meanvaluetheorems,
- · Taylorseries,
- · Theoremsofintegralealculus,
- · Multipleintegrals,
- · Evaluation of definite and improper integrals,
- Surfaceandvolumeintegrals,
- · Partialderivatives,
- · Line.

ComplexAnalysis:

- · Cauchy'sintegralformula,
- · Analyticfunctions,
- · Residuetheorem,
- · Cauchy'sintegraltheorem,
- · Taylor'sandLaurent'sseries.D

ifferentialEquations:

- · Particularintegral&Complementaryfunction,
- · Firstorderequations(nonlinearand linear),
- · Initial&boundaryvalueproblems,
- · Higherorderlineardifferentialequations,
- · Partialdifferential equations,
- · Cauchy's&Euler'sequations,
- Variableseparablemethod,
- Methodsofsolutionusingthevariationofparameters.Nu

mericalMethods:

- · Single&Multi-stepmethodsfordifferentialequations,
- Convergencecriteria,
- Solutionofnonlinear equations.

GAESyllabusforEEE-Networks, Signals and Systems

- Networksolutionmethods:
 - · SolutionofnetworkequationsusingLaplacetransform,
 - Nodalandmeshanalysis,
 - · Stateequations fornetworks,
 - · Timedomainanalysisofsimplelinearcircuits,
 - · Networktheorems:
 - · Superposition,
 - Maximumpowertransfer
 - TheveninandNorton's.

- · Frequency domain analysis of RLC circuits,
- · Wye- Delta transformation,
- · Linear2-portnetworkparameters:
 - · Driving point and
 - Transfer functions.
- · Steady state sinusoidal analysis using

phasors

- · Continuous-time signals:
- Discrete-timesignals:Z-transform,Discrete-timeFouriertransform(DTFT),Interpolationofdiscrete-time signals,FFT, DFT.

Fourier series and Fourier transform representations ,LTI systems:

- · Poles and zeros,
- · Definition and properties,
- · Digital filter design techniques,
- · Causality,
- · Parallel and cascade structure,
- · Stability,
- · Phase delay,
- Impulse response,
- Frequency response.

Syllabus of GATE EEE 2017-18-Electronic Devices

- BJT,
- Energy bands in intrinsic & extrinsic silicon,
- Integrated circuit fabrication process:
 - · Ion implantation,
 - · Oxidation,
 - · Photo lithography &twin-tub CMOS process,
 - Diffusion. Carrie transport:
 - · Resistivity,
 - · Diffusion current,
 - Mobility, and
 - · Drift current.

MOS capacitor,

Generation and recombination of carriers ,Photo diode and Solar cell, Poisson and continuity equations ,MOSFET,P-N junction, LED Zener diode.

GATE Syllabus for EEE 2017-18 -Analog Circuits

- · Active filters,
- Small signal equivalent circuits of diodes,
- Power supplies:
 - · Ripple removal, and
 - · Regulation.

BJTs and MOSFETs

.Sinusoidal

oscillators:

- Criterion for oscillation,
- Single-transistor & op-amp configurations.
- Simple diode circuits:
 - · Clamping,
 - · Clipping, and
 - Rectifiers

Voltage reference circuits,

Single-stage BJT and MOSFET amplifiers:

- · Biasing,
- Mid-frequency small signal analysis,
- Bias stability, and
- Frequency

response.

Function

generators,

BJT and MOSFET amplifiers:

- Multi-stage,
- Differential,
- · Feedback,
- Power & operational.

Wave-shaping circuits and 555 timers, Simple op-ampcircuits.

GATE2017-18EEESyllabus-DigitalCircuits

- Data converters:
 - · ADCs and DACs,
 - Sample &hold circuits.

Number systems,

Combinatorial circuits:

- · Code converters,
- · Boolean algebra,
- · Decoders and PLAs,
- · Arithmetic circuits,
- Minimization of functions using Karnaugh map & Boolean identities, Multiplexers,
- · Logic gates & their static CMOS implementations.

Semiconductor memories:

- · ROM,
- · DRAM,
- · SRAM.

Sequential circuits:

- · Shift-registers,
- · Latches & flip-flops,
- · Finite state machines,
- Counters.

GATE Exam Syllabus EEE 2017-18 - Control Systems

- Transient & steady-state analysis of LTI systems,
- Basic control system components,
- Lag, lead & lag-lead compensation,
- Frequency response,
- · Feedback principle,
- · Bode and root-locus plots,
- State variable model,
- Transfer function,
- · Solution of state equation of LTI systems,
- Block diagram representation,
- Routh-Hurwitz and Nyquist stability criteria,
- Signal flow graph.

GATE Syllabus for EEE 2017-18 -DC MACHINES

- · Basics of DC machines.
- Introduction to electric drives/
- Introduction to measurements, types of MI
- Parts of dc machines, working of DCMK



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DETAILED REPORT ON CONDUCTION OF GATE CLASSES (2017-18)

GATE exam has gained a lot of Importance as students who qualify GATE are eligible for direct recruitment in PSUs like BPCL, ONGC, BARC, NTPC, NPCIL, GAIL, BHEL, DRDO, IOCL, NALCO,

CtC.HOD EEE visited all the final year EEE classes and highlighted the importance of GATE exam for PSUs as well as higher studies. This improved the enrolment ratio from around 45% in year 2013-14 to around 72% in consecutive years. GATE (2017-18) Classes have been handled for IV EEE Students from 04/10/2017 for 2013 admitted batch students and 8 Subjects have been handled by different faculty as stated In the list and they covered the topics from previous gate papers. Training of 60 hrs along with 4 to 5 mock test is scheduled for students appearing GATE 2018. The students participating in GATE Training were also provided with the entire set of notes consisting of Important topics and useful for further preparation.

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GATE 2018

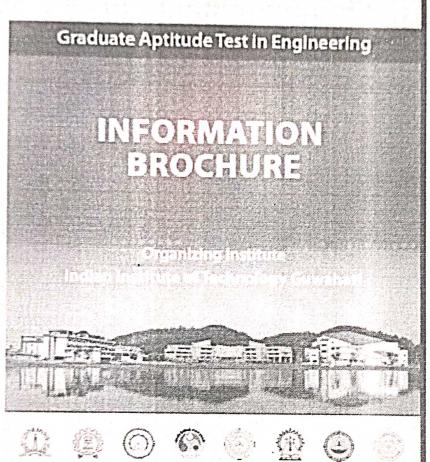


Table 3.1 Important Dates related to GATE 2018

GATE Online Application Processing System (GOAPS) Website Opens	Friday	Old September 2017
Last Date for Submission of (Online) Application (through Website)	Thursday	05th October 2017
Last Date for Requesting Change of Examination City (an additional fee will be applicable)	- Friday	17 th November 2017
Admit Card will be available in the Online Application Portal (for printing)	Friday	05th January 2018
GATE 2018 Examination Forenoon: 9:00 AM to 12:00 Noon Afternoon: 2:00 PM to 5:00 PM	Saturday Sunday Saturday Sunday	03% February 2018 04% February 2018 10% February 2018 11% February 2018
Announcement of the Results in the Online Application Portal	Saturday	17 th March 2018