International Conference on Electrical, Communication, Electronics, Instrumentation and Computing (ICECEIC) - 2019

30th & 31st January- 2019

Conference Proceedings by

IEEE Xplore® Digital Library

Organized by

Sri Chandrasekharendra Saraswathi Viswa Mahavidyalaya

Sri Jayendra Saraswathi Street, Enathur,
Kanchipuram, Tamil Nadu, India - 631 561.

ISBN: CEPr9R88-PRT 978-1-7281-0173-6

Supported by

IEEE Advancing Technology for Humanity

IEEE Madras Section

CPGC

CSTPLI

page-126, page-165, 166.

International Conference on Electrical, Communication, Electronics, Instrumentation and Computing (ICECEIC) - 2019

455, 355

Issue - I

30th & 31st January 2019

IEEE Conference Proceedings

Organized by

Sri Chandrasekharendra Saraswathi Viswa Mahavidyalaya College

Kanchipuram, Tamil Nadu, India.

ISBN: CFP19R88 - PRT: 978-1-7281-0173-6

Supported by

IEEE Advancing Technology for Humanity

Technical Sponsor by IEEE MADRAS Section

CPGC

CSTPLI

Performance of MIMO-OFDMA system using STBC-MRC in different fading Channels

Smt. D.Lalitha Kumari and Dr. M.N.Giri Prasad

Abstract:Multiple-Input Multiple-Output (MIMO) Combined with Orthogonal Frequency Divisi Multiple Access (OFDMA) is regarded as a promising solution for enhancing the performance of ne generation wireless systems. This framework of such system is called as MIMO-OFDMA system. this paper, we investigate MIMO-OFDMA system with Space Time Block Coding (STBC) as transm diversity and Maximal Ratio Combining (MRC) as receiver diversity in different multipath fadi channels such as Rayleigh, Rician and Weibull Channels. This OFDMA system designed based on t standard characteristics of Worldwide Interoperability for Microwave Access (WiMAX). Th Simulation results show Bit Error Rate (BER) performance for different antenna configurations.

Impedance Based Stability Criterion for Grid-Tied 3-Ø Inverter through LCL-Filter

P.Vinod kumar and G.Jagadeesh

Abstract:The main objective of this paper is to give an idea on Impedance Based Stability Criteric (IBSC) for Grid Tied 3-Ø Voltage source inverter because the grid tied inverter become unstable whe the grid impedance is high (if the Load on the grid increase then the reactance of the grid increas through cross the operating point of the grid impedance), A Current research method (IBSC) is used analyse and determine the stability (operating points) of the grid tied inverter in distributed powe system by using inverter output impedance and grid impedance, here the grid tied inverter will remai stable if the ratio of grid impedance to inverter output impedance must satisfies the frequency domai stability criterion(Nyquist (or) Inverse nyquist) and this approach is applicable for voltage-source an current-source systems.

A Delay Adjustable Power ON Reset Circuit

Akhila Punaroor and ShashidharTantry

Abstract:In this paper we have designed Power ON Reset (POR) circuit with adjustable delay. Mai intent of this project is to generate a pulse for ramping power supply. The delay is adjustable by addin or removing transistor capacitor to the circuit. We have used transistor as capacitor so that we ca reduce the size of circuit. A POR circuit having an adjustable delay is proposed. The circuit has bee designed in CMOS process to work for a supply voltage ranging from 1.8V-3.3V. The circuit generate a POR signal after a known delay, after the supply voltage crosses certain threshold voltage. Th proposed circuit is designed and simulated in Cadence Design Environment with GPDK180nm technology.