DESIGN OF NEW LOW-POWER AND AREA EFFICIENT FULL ADDER FOR ARITHMETIC APPLICATIONS

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Abstract—***In many computers and processors, adders are used to calculate addresses, similar operations and table indices in the ALU and also in other parts of the processors.Presenting high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles with reduced complexity and energy efficient. The proposed full adder is compared with other full-adders reported as having a low PDP, in terms of speed, power consumption and area. The simulations are carried out in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology. From this it is evident that with the proposed full adder design there is 55.5% in delay and 35.5% reduction in power dissipation.***

Keywords—***Inverter, Half adder, XOR, XNOR, PASS Transistor.***

Introduction

In various microprocessors and application specific DSP architecture addition, subtraction are basic arithmetic operations. In addition the main task is to add two numbers, as it is also used in many other useful operations such as address calculation, subtraction, multiplication, etc.

The full adder are designed with fewer transistors to save chip area does have excellent performance. Some full adders are designed to emphasize making up for threshold voltage loss to improve circuit performance where Energy-efficiency is said to be one of the most required features in modern electronic systems designed for portable applications and/or high-performance. The module used is the core of many arithmetic operations like Addition and Subtraction etc [1]. The PDP can taken this fact into consideration that the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital design systems. In this paper, we have been reported that the comparison, performance and design of three full-adder cells implemented with an alternative internal logic structure, depends upon multiplexing of the Boolean functions like XOR/XNOR and AND/OR, in order to reduce power consumption several CMOS logic styles have been evolved for the developing of the cell libraries. As they are willing to immortalize the ability and to further reduce the cost-per function and improve the performance of integrated circuits [3]. By lowering the threshold voltage in ultra deep submicron technology, low supply voltage appears to be most eminent has to reduce power consumption. The resultant full-adders showed more efficiency in terms of power consumption and delay when compared with other previously reported to build low-power arithmetic modules.

BASIC FULL-ADDER

Digital Adder is a device which is capable of adding two digital n-bit binary numbers, where value of 'n' depends on the circuit implementation. A full adder is a logic circuit which performs an addition operation on three one-bit binary numbers. The full adder produces a sum of the inputs and carry value.

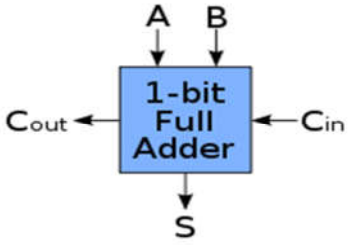

Fig : Full adder block diagram

Some other multi-bit adder architectures breaks the adder into blocks. It is possible to vary the length of these blocks based on the propagation delay of the circuit to optimize computation time [2]. These type of adders include the carry bypass adder which determines P and G values for each block rather than each bit, and the carry select adder pre-generates sum and carry values for carry input to the block.

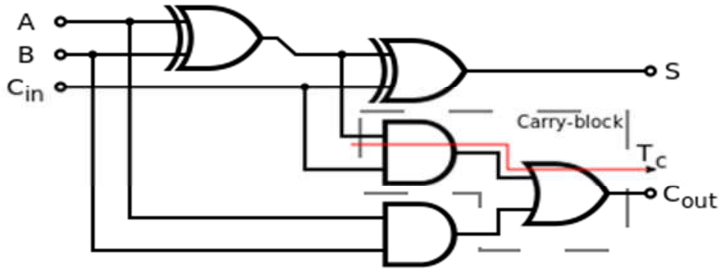

Fig: Full adder logic diagram

Full adder can also be constructed using two half adders by connecting A and B to the input of one half adder and sum that to an input to the second adder, connecting C_i to the other input and OR to the two carry outputs. Equivalently, S could be made the three-bit XOR of A, B, and C_i, and C_o could be made the three-bit majority function of A, B, and C_i.

I. REVIEW OF EXISTING LOGICS

A.INVERTER

The schematic of inverter circuit is shown in below figure 1.The operation of the inverter circuit is as follows: Initially, the CMOS inverter is assumed to be operated in a steady state, having input as logic HIGH and hence at output the logic LOW is present. In this case the output capacitor is discharged. When the input waveform undergoes a falling transition, the p-MOS transistor will be (ON) and the corresponding n-MOS transistor turn off [4]. The current drawn from the power supply charges the capacitor C_L up to V_{dd}. During this charging process, the energy drawn from the power supply is $C_L.V_{dd}^2$,out of which half is stored in the capacitor C_L and the other half is dissipated from the parasitic capacitances of p-MOS transistor and the interconnect. When the input waveform undergoes a rising transition, the n-MOS transistor conducts and the p-MOS transistor turn off [12].

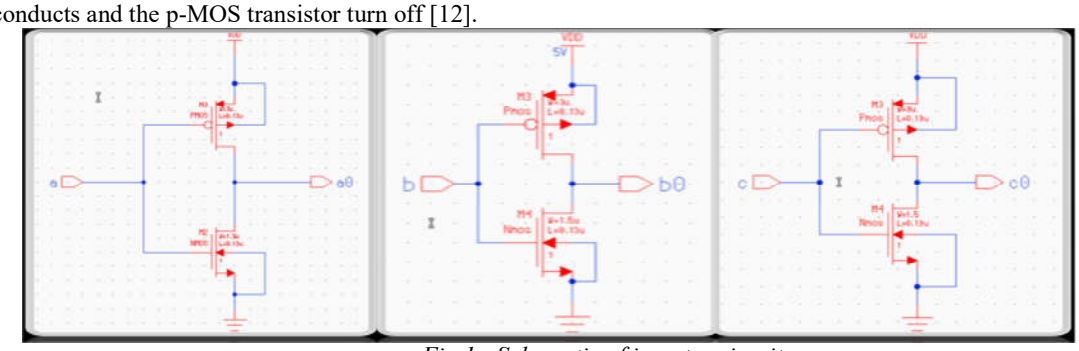

Fig 1: Schematic of inverter circuit

B.DOUBLE-PASS TRANSISTOR LOGIC

The other new full-adder have been designed using the logic styles DPL , and the new logic structure presents a full-adder designed with DPL logic style as shown in figure 2 and figure 3 are used to build XOR/XNOR gates and a pass-transistor based multiplexer used to obtain the So output. These SR-CPL and other logic styles were used to build XOR/XNOR gates. In both the cases, the AND/OR gates have built using powerless and groundless pass-transistor configuration respectively, and a pass-transistor based multiplexer is used to get the Co output [7].

Double-pass transistor logic eliminates some of the inverter stages which are required for the complementary pass transistor logic by using both N and P channel transistors, with dual logical paths for each function. Though it has high speed operation due to low input capacitance[11]. The switching tree of a DPL gate consist of both NMOS and PMOS pass transistors, in contrast with the switching tree of an CPL gate. The full swing operation is attained by simply adding PMOS transistors in parallel with the NMOS transistors. The switching tree of a CPL gate consists of only NMOS transistors, which results in a lower input capacitance [8]. The full-swing output-voltage restoration of an DPL-gate can be done by using the combination of an NMOS and a PMOS transistor, instead of the PMOS-latches and inverters. These are used by means of the Complementary Pass Transistor (CPL) logic. Double pass-transistor logic (DPL) uses both PMOS as well as NMOS devices in pass-transistor network to avoid non full swing problems, but it is having high-power and high-area drawbacks [5].

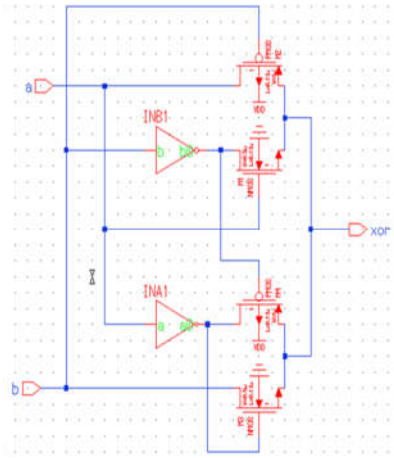

Fig 2: XOR Schematic Using Dpl Logic Style

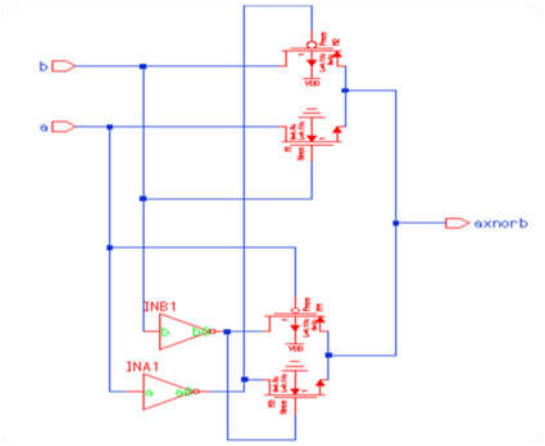

Fig 3: XNOR Schematic Using Dpl Logic Style

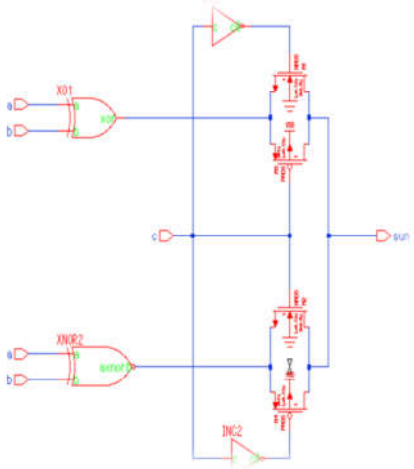

Fig: Sum Schematic Using Dpl Logic Style

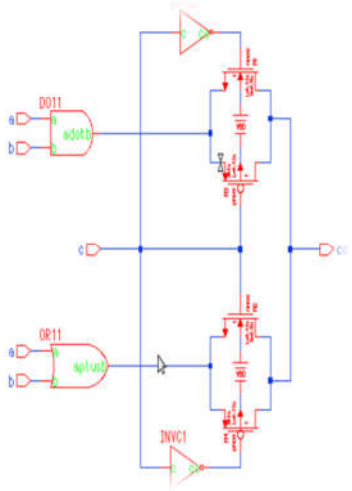

Fig: Carry Schematic Using Dpl Logic Style

C. SWING RESTORED PASS TRANSISTOR LOGIC

Many designs have been implemented for the optimization of low-power full-adders, trying different options for the logic styles double pass-transistor logic (DPL), swing restored CPL (SR-CPL) and the logic structure used to build the adder module[6]. The enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate as shown in figure 4 and figure 5. The SR- CPL schematic, the simulation of this environment has been used for compiling full adders' analyses within the addition of the inverters at the outputs. The size of the input buffers are degradation in the input signals, and the size of the output buffers equals to the load of 4 small inverters for this technology.SR-CPL is very similar to CPL, because it uses the same NMOS pass-transistor network [9].

The complementary pass-transistor logic or Differential pass transistor logic refers to a logic family which is designed for definite advantages. In this the CPL logic uses a series of transistors for selecting the possible inverted output values of the logic in which output can be used to drive an inverter and to generate non-inverted output signals with inverted and non-inverted inputs which are required to drive the gates of the pass-transistors. The main concept behind this CPL is the use of an NMOS pass-transistor network for purpose of logic organization. The CPL concept consists of complementary inputs/outputs and NMOS pass-transistor logic network, CMOS output inverters [10].

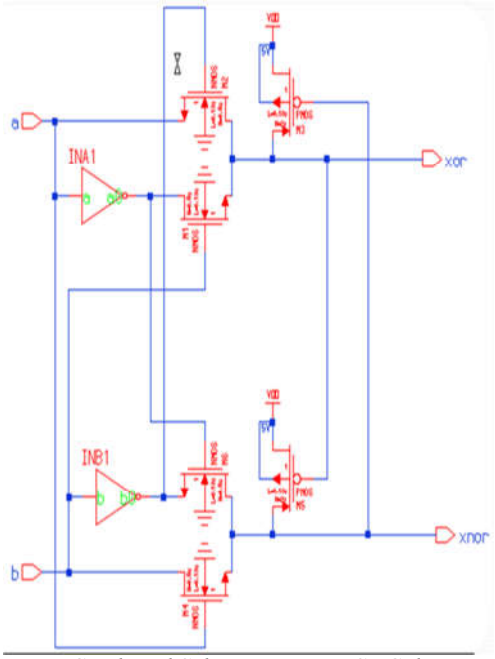

Fig 4: Combined Schematic Using Sr-Cpl Logic Style

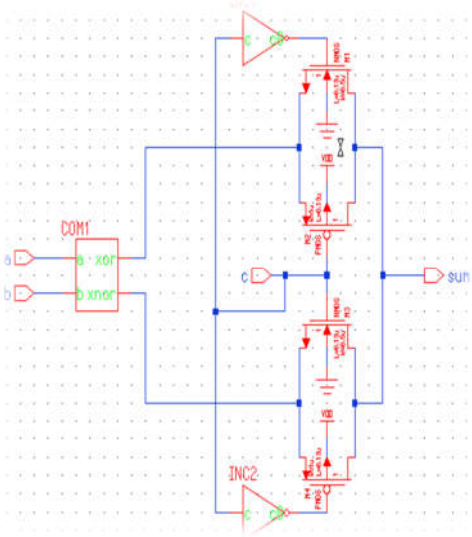

Fig 5: Sum Schematic Using Sr-Cpl Logic Style

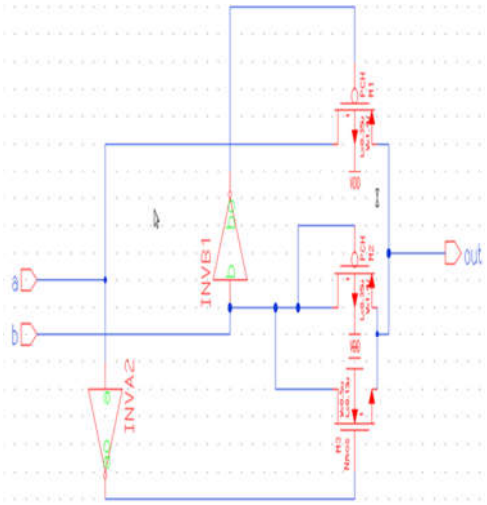

Fig: OR Schematic Using Sr-Cpl Logic Style

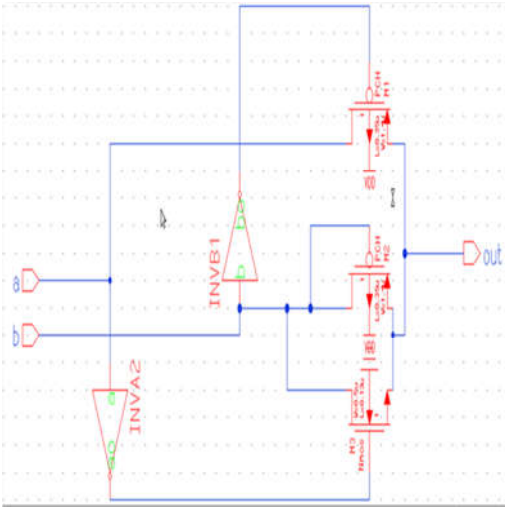

Fig: AND Schematic Using Sr-Cpl Logic Style

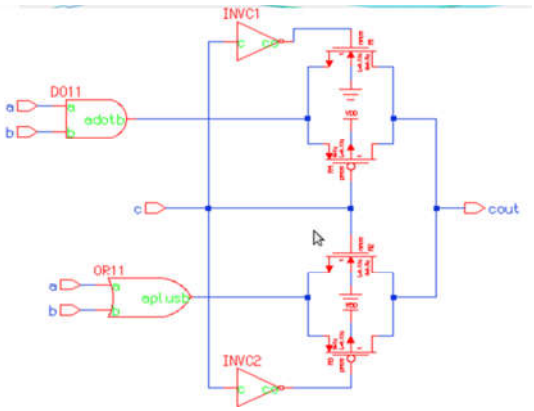

Fig: CARRY Schematic Using Sr-Cpl Logic Style

II. PROPOSED LOGIC

A. PASS TRANSISTOR LOGIC

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits .Basically it reduces the number of transistors count which used to make different logic gates simply by eliminating redundant transistors as shown in figure 6 and figure 7. These type of transistors are used as switches to pass logic levels between the nodes of an circuit, instead of using switches to connect directly to supply voltages. Which in turn reduces the number of active devices, but has the disadvantage in this circuit is that the difference between the voltages between high and low logic levels decreases at each stage. Each transistor which is connected in series is less saturated at its output when comparing it with the value at its input [5]. By contrasting conventional CMOS logic switched transistors, the output connects to one of the power supply rails, so that the logic voltage levels in a sequential chain do not decrease. Since there will be less isolation between input signals and outputs, so the designers must take care to assess the effects of unintentional paths are within the circuit. For proper operation, the design rules restrict the arrangement of circuits so that the sneak paths, charge sharing, and slow switching can be avoided.

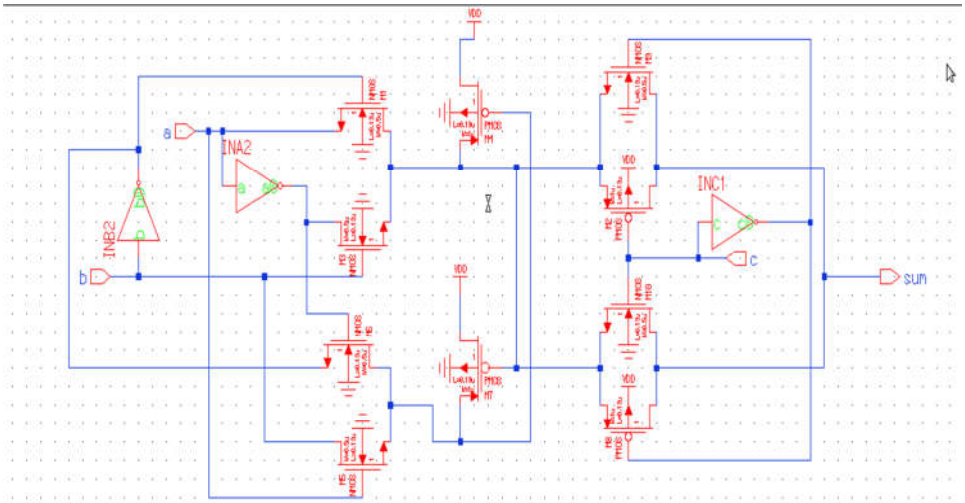

Fig 6: Sum Schematic Using Pass Transistor Logic Style

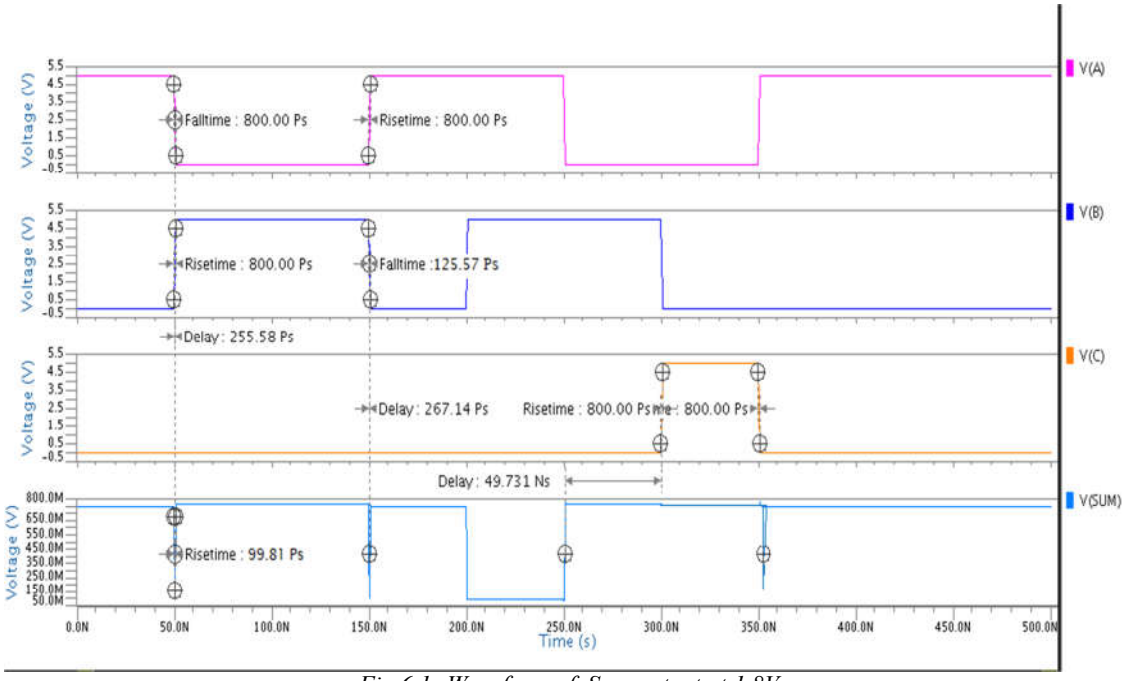

Fig 6.1: Waveform of Sum output at 1.8V

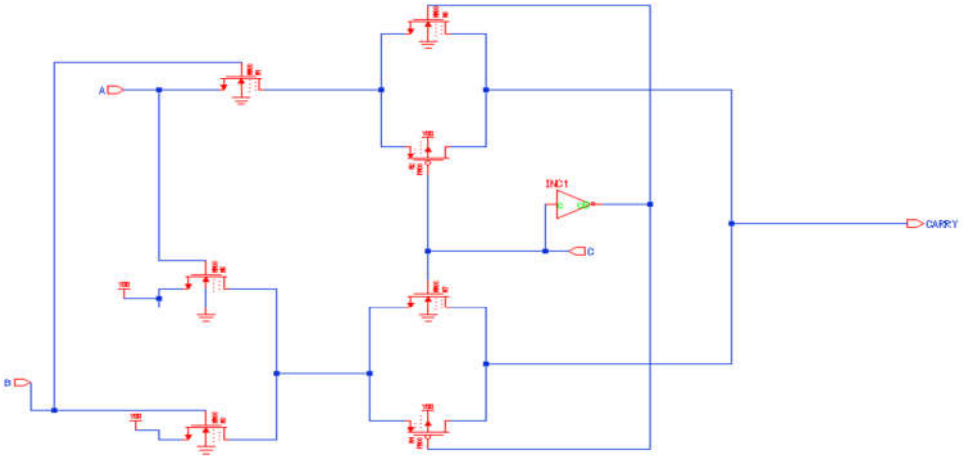

Fig 7: Carry Schematic Using Pass Transistor Logic Style

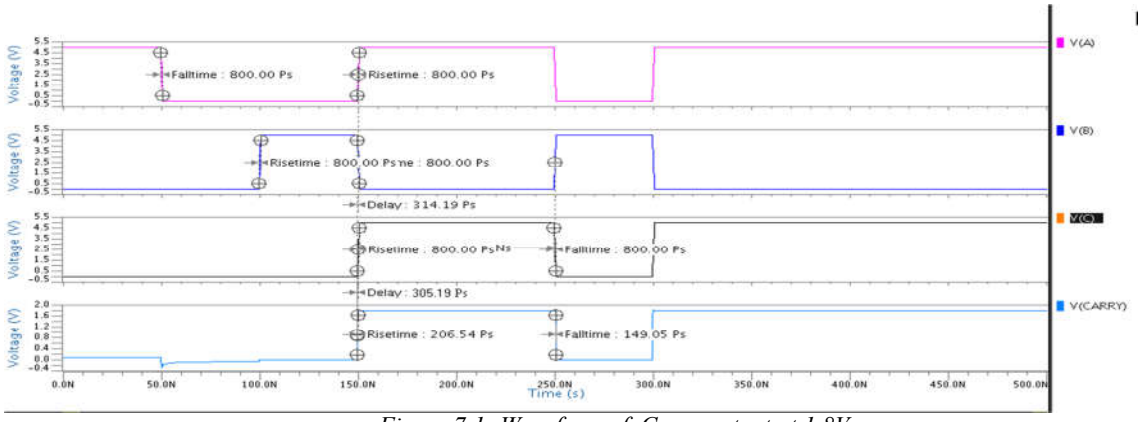

Figure 7.1: Waveform of Carry output at 1.8V

III. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

All the full adder simulations were designed using Semiconductor Limited's Generic 0.13µm CMOS technology, at a supply voltage of 1.8V, using MENTOR GRAPHICS TOOL. The performance of the proposed full adder is evaluated and compared with existing full adders. Below table summarize the performance of the reviewed existing full adders and proposed designs.

S.NO	LOGIC USED	OUTPUT TYPE	NO. OF TRANSISTORS USED	RISE TIME	FALL TIME	DELAY	POWER DISSIPATION
1.	DPL	SUM	18	97.873 PS	266.74 PS	357.74 PS	5.5530 NW
		CARRY	16	113.39 PS	211.24 PS	291.74 PS	4.3626 W
2.	SR-CPL	SUM	16	95.046 PS	114.56 PS	334.25 PS	4.192 NW
		CARRY	16	110.12 PS	168.27 PS	291.19 PS	475.317 NW
3.	PASS TRANSISTOR	SUM	16	99.81 PS	125.57 PS	314.27 PS	1.0290 NW
		CARRY	13	206.54 PS	149.05 PS	305.19 PS	502.714 PW

IV.APPLICATIONS

Comparators are the key design elements for a wide range of applications such as:

- To calculate addresses.
- To calculate increment & decrement operators.
- Arithmetic logic units or ALU operations.
- Ripple Carry Adder
- Carry Look Ahead Adder

V.CONCLUSION

In this Paper, a new high performance and power efficient full adder using multiplexer based pass transistor logic is designed. Further an alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were realized by using different logics styles are DPL, SR-CPL. So, the required logic can be realized by using an optimized area which performs faster when compared to the conventional static CMOS full adder design. Pre-layout simulation results in 0.13-μm CMOS technology confirmed that the optimized area and power dissipation of the proposed full-adder is reduced to a great extent and performs faster when compared to the existing CMOS full adder design.

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