IMPLEMENTATION OF AREA EFFICIENT SRAM CELL WITH 130nm CMOS TECHNOLOGY

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ABSTRACT

Different circuits are available in the design of SRAM cell. The standard SRAM cell consist of 6 transistors in which two CMOS inverters are connected back to back and other two are access transistors . The main parameters that are focused under the design of a 6 transistor SRAM cell are read noise margin, write noise margin, read stability, write stability, power consumption etc., this 6 transistor SRAM cell consumes very less power and requires very less read and write time. As stability and area are the major concerns in SRAM cell design, the aim is to design an area efficient SRAM cell. The proposed SRAM cell consists 3 transistors which consists a transmission gate to stores the bit of information and on access

transistor. This will be achieved by reducing the number of transistors in SRAM cell design. If the number of transistors reduced, increases the area efficiency, intern reduces the power consumption of the memory cell. The proposed SRAM cell will be designed, implemented and analysed in standard technology library called Pyxis of 130nm technology using mentor graphics tool.

Key words: SRAM cell, Low power, Area efficient.

INTRODUCTION:

The scaling of CMOS IC technologies made the manufacture of faster and smaller circuits which in the case of SRAM memories has resulted in larger storage capacity and shorter access-time. Some percentage of the total area of current System-on-Chip (SoC) is dedicated to memory blocks. One consequence of this fact is that embedded SRAM dominates the overall performance. However, with small device dimensions, design rules, and the ever-increasing demand for on-chip cache capacity, the standard 6 transistors cell (6T-cell) has less effect on functional failures. SRAM cell size continues to decrease by half each generation. Despite scaling, SRAM cells must be stable during read and write operations. The most important parameters that are mainly considered are threshold voltage, variability, implying that design rules are generally adapted to accommodate power, performance, and area restrictions.

Cell stability during read operations is increased by strengthening the internal latch inverters and weakening the access transistors, while the opposite is desired for cell write-ability: a weak inverter and strong access transistors must be chosen such that read stability and write-ability are both within reasonable levels. Based on these constraints it is usually assumed that the pull-down transistors of the internal latches of SRAM cells, must be wider than the access transistors, while the access transistors should be not too small compared with the pull-up transistors (usually they are equal sized).

The total cell area is dominated by these two constraints. In this paper we investigate the possibility of using minimum size transistors to achieve area efficiency of a 2transistor cell when compared to conventional 6T and 4T by maintaining stability of an SRAM cell within acceptable values. The study includes electrical simulations as well as experimental measurements from SRAM devices fabricated in a 130 nm CMOS technology on a Pyxis tool of mentor graphics.

REVIEW OF EXISTING CELLS:

1.6T SRAM CELL:

The basic SRAM cell consists of six transistors. The basic schematic is as follows:

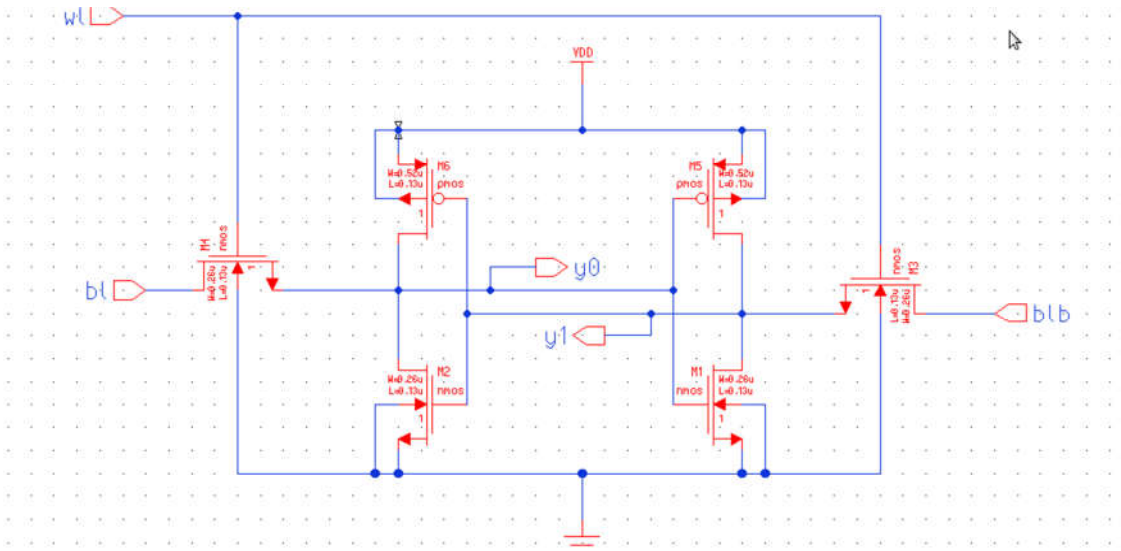

Figure1: schematic circuit of 6 transistor SRAM cell

The generic structure of MOS static RAM cell, consisting of two cross coupled inverters and two access transistors. The two access transistors are controlled by the word line connecting bit lines (BL and BLB) with the internal nodes Y0 and Y1. The two back-to-back connected inverters forms a latch.

The 6T SRAM cell mainly performs three operations

- Standby mode
- Read operation
- Write operation

Standby mode:

If the word line is not asserted, the access transistors should disconnect the cell from the bit lines. The two cross-coupled inverters formed will continue to reinforce each other as long as they are continued to the supply.

Write operation:

In a write operation, the word line connected to access transistors turns on (WL=1).

The requirement to perform a write operation is met by setting the pull-up ratio (PR= Wp/Wacc) usually lower than 3. To minimize cell area, the size of the pull-up and pass transistors are typically chosen to minimum. Obviously, the 6T-MSC cell also has PR=1.

For performing write operation , the input data is sent through the bit lines BL and BLB and the output is taken across Y0 and Y1.The data that is given as an input to the bit lines will make the corresponding transistors ON and OFF according to the input given. If the input is 0, the NMOS transistors will turn OFF and PMOS transistors will turn ON and vice-versa.

s.no	Parameters	Value

Read operation:

In a read operation, the word line that is connected to the access transistor turns on (WL=1).

In a read operation, the pre-charged bit-lines disturbs the "0" storage node, through the access transistor, by pulling it up. To guarantee a non-destructive read, the cell ratio CR (also known as β ratio), defined as CR=Wn/Wacc, is usually comprised between 1.5 and 2.5.

For performing read operation, the bit lines BL and BLB are output nodes. Firstly, the bit lines are precharged upto Vdd and the corresponding NMOS transistors will ON and PMOS transistors will OFF. The obtained output is taken across bit lines and it is read from the memory.

Simulation results:

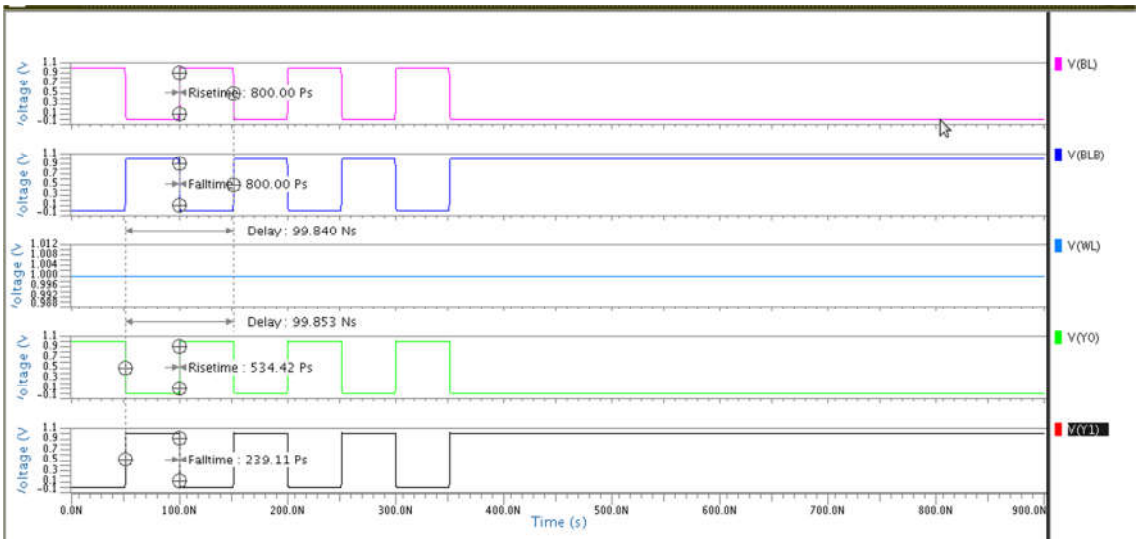

Figure2:simulation waveform

Limitation in 6T SRAM cell:

The read stability in SRAM cell should be occur when the cell ratio is comprised between 1.5 - 2.5. In a 6T SRAM cell, the cell ratio is 1. There may be a chance of effecting read stability. This is the major limitation in 6T SRAM cell.

The limitation in 6T SRAM cell is avoided by reducing the transistor count i.e. the memory cell is constructed by using four transistors.

Result analysis:

The different parameters like Rise time, fall time, Delay, Power dissipation are calculated from the simulation waveform.

1	Rise time	800.00ps
2	Fall time	239.11ps
3	Delay	998.53ps
4	Power dissipation	1.2441N watts

2.4T SRAM CELL:

Like 6T SRAM cell, it also have a cross coupling connection between two transistors but not between two inverters

In addition to these transistors which are cross coupled, another two NMOS access transistors are connected by word lines. The word lines are also known as address lines. These lines provide access to the inverters whey they are performing read and write operations. The one terminal of NMOS access transistors are connected to bit lines which are complementary to each other. The word lines are represented with WL and two complemented bit lines are represented with BL and BLB. The bit lines are also known as data lines. These data lines and address lines are responsible for the operations performed in the SRAM memory cell.

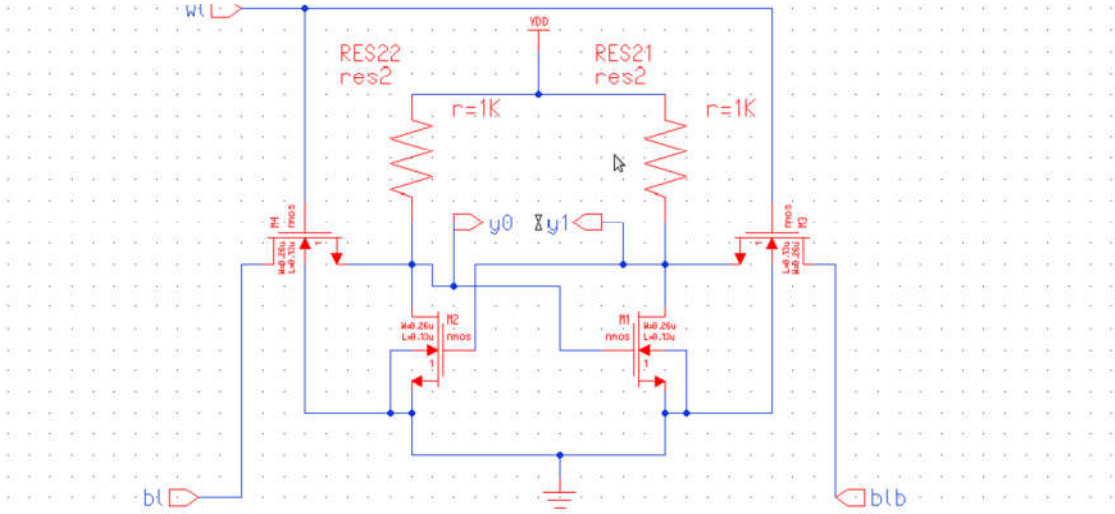

Figure3: schematic circuit of 4 transistor SRAM cell

To perform read and write operations, two NMOS pass transistors are used. Note that the SRAM cell is accessed by two bit lines or columns, instead of one. This complementary column arrangement allows for a more reliable operation.

When the word line is not selected i.e., when the voltage level of line is equal to logic ‘0’, the pass transistors are turned off. The simple latch circuit consisting of the two cross-coupled inverters preserves one of its two stable operating points, hence data is being held. At this point, consider the columns (bit lines). If all the word lines in the SRAM array are inactive, the relatively large column capacitances are charged up by the column pull-up transistors.

Since both transistors are operating in saturation, the steady state voltage level Vc for both columns is determined by the following relationship:

$$\text{Vdd-Vc=Vto+}(\sqrt{|2\varphi f|} + Vc - \sqrt{|2\varphi f|}$$

Simulation results:

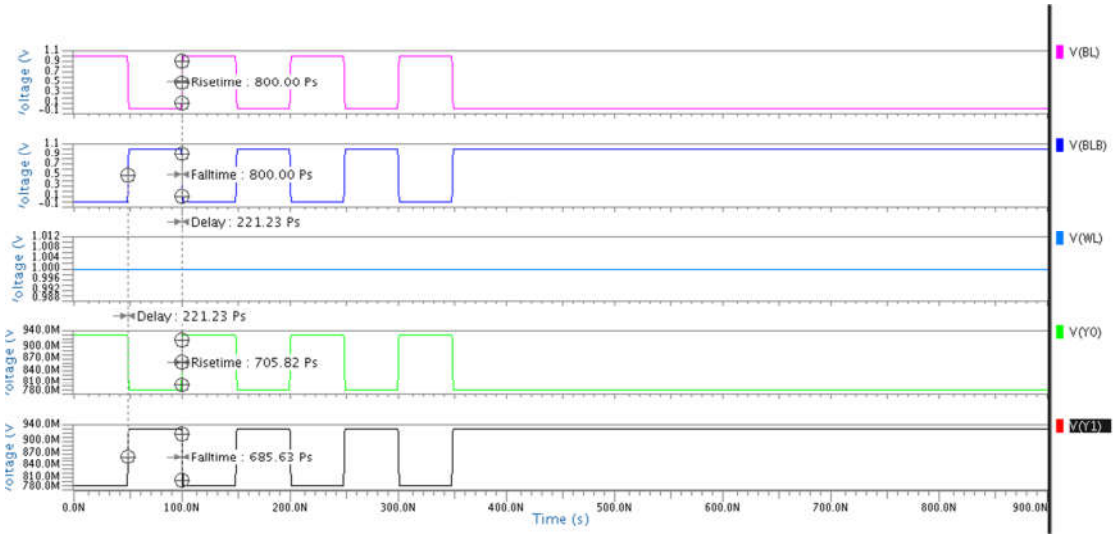

Figure4: simulation waveform

Limitations of 4T SRAM cell:

- As the 4T SRAM cell is provided with resistors it gives rise to voltage drop that will lead to leakage currents. This is the great disadvantage to SRAM cell. It may result in the variations of read and write operations of the cell.
- Each cell has current flowing in one resistor i.e., the SRAM has a high standby current.
- The cell is sensitive to noise and soft error because the resistance is so high.
- The cell is not as fast as the 6T SRAM cell.

Result analysis:

The different parameters like Rise time, fall time, Delay, Power dissipation are calculated from the simulation waveform.

s.no	Parameters	Value
1	Rise time	705.82ps
2	Fall time	685.63ps
3	Delay	221.23ps
4	Power dissipation	279.6409U watts

3.2T SRAM CELL:

A new SRAM cell constructed with 2 transistors is designed and implemented. In this ,there is an NMOS driver transistor and a PMOS load transistor of. Data is stored on the interconnection of both the transistors at Q. NMOS Driver transistor works as access transistor also. Gate input of NMOS connected to WL line provide access to 2T cell during read and write operations. In this circuit a single bit line BL is used for 2 bit lines in 6T and 4T cell. Since 2T cell requires single bit line the pre charge and sense amplifier are also single ended. Charge stored in the bit line BL drives the sense amplifier and determine the logic value at the output Y. Cell area is greatly reduced by 66% without affecting the working.

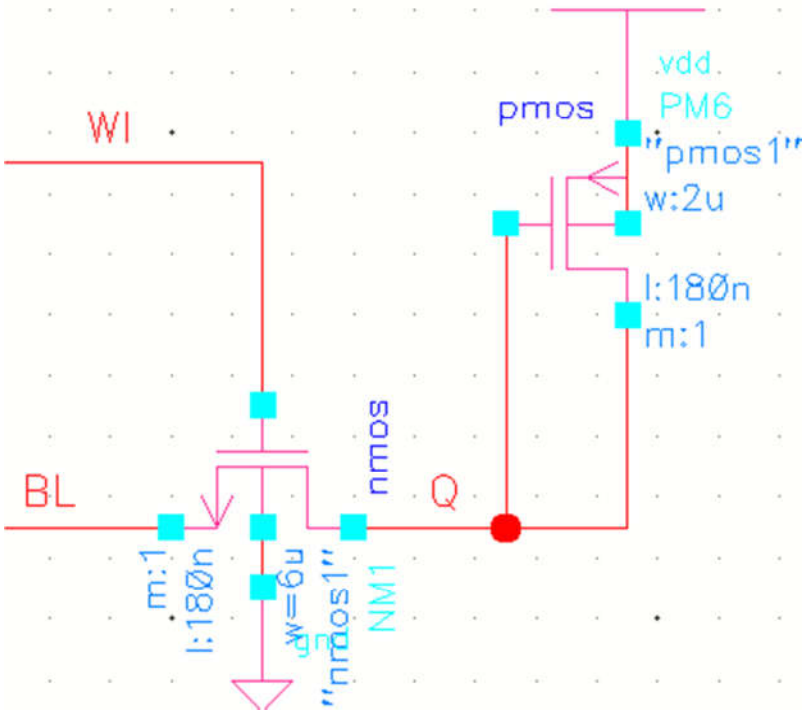

Figure5: schematic circuit of 2 transistor SRAM cell

For write operation, the data has to be placed on BL and turn on NMOS driver transistor. If data is “1”, WL turns on access transistor which makes Q to 1 (Vdd-Vth). If data is “0” node Q finds a direct path to ground. Charge stored on node Q discharges through driver transistor. Load transistor then discharges to ground through node Q and maintains low voltage at node Q.

To maintain charge on node Q , the driver transistor should be 3times wider than that of load. In this case there is a direct path from Vdd to ground which is going to increase power. Read cycle is started by enabling SE signal, voltage on BL sensed by sense amplifier

For 2T cell, read cycle finds a direct path from supply to ground it greatly increases the dynamic power. Power consumption in 2T SRAM memory cell is very much greater than other memory cells. If data on node Q is ‘1’ it turns off PMOS node discharges

through driver transistor but when data on node Q is '0' it turn on PMOS and PMOS stays on which leads to power consumption. One extra read1 cycle required to reduce power consumption.

Simulation results:

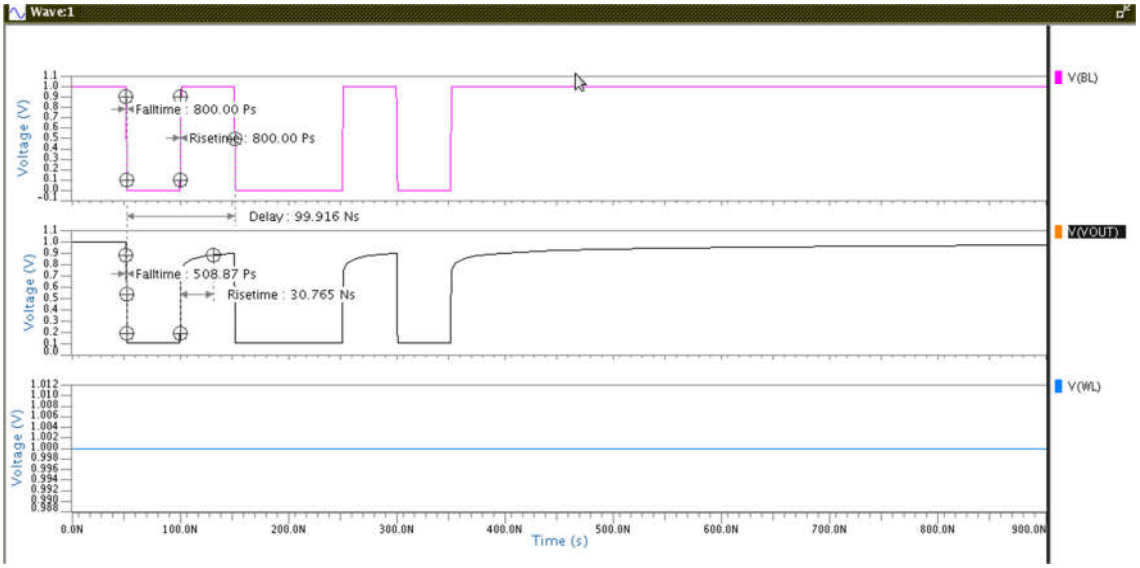

Figure6:simulation waveform

Limitations of 2T SRAM Cell:

- The major limitation in 2T SRAM cell is for both read and write operations there is a common storage point
- Power consumption is more in 2T SRAM cell when compared to other configuration SRAM cells

Result analysis:

The different parameters like Rise time, fall time, Delay, Power dissipation are calculated from the simulation waveform.

s.no	Parameters	Value
1	Rise time	307.65ps
2	Fall time	508.87ps
3	Delay	999.16ps
4	Power dissipation	2.0009N watts

PROPOSED 2T SRAM CELL:

The designs what we are discussed till now are all designed and implemented by different methods. Now we are doing different approach that is based on the criteria that the main aim to modify the design is to improve the area efficiency

We suppose that the proposed design consists of two NMOS transistors connected back to back ad there are no PMOS transistors. The main aim to design the cell with two NMOS transistors is to avoid storage problem in the already designed 2T SRAM cell.

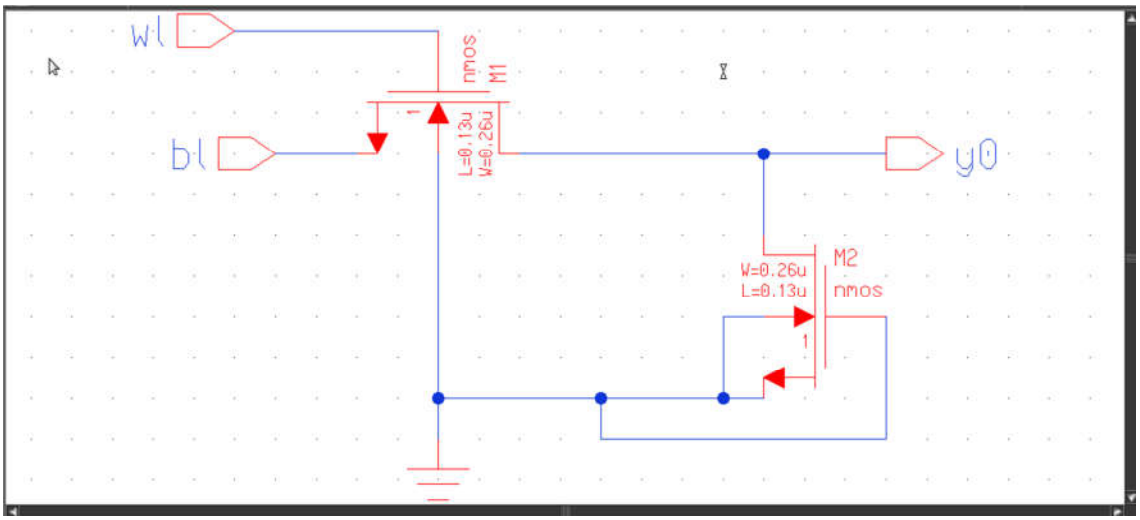

Figure7: schematic circuit of proposed 2T SRAM cell

The modified design consists of two NMOS transistors. One NMOS transistor gate and drain regions are connected to word line and bit line and source region of same transistor and source region of another transistor are connected to the output denoted by y0. The word line is denoted by wl and bit line is denoted by bl. The substrates of both the transistors are connected to ground and gate of the second transistor is also connected to ground. This type of modification for the already designed 2T SRAM cell will may overcome the limitation of charge storage in the predefined 2T SRAM cell. Especially, in 2T SRAM memory cell, there is a storage node which is represented by Q is responsible for read and write operations. The output is taken across the storage node Q. At the storage node, the drain terminal of the NMOS transistor and the gate terminal of the PMOS transistor are combined and at this particular point the two values both logic ‘1’ and logic ‘0’. This is a great disadvantage in 2T memory cell.

Simulation results:

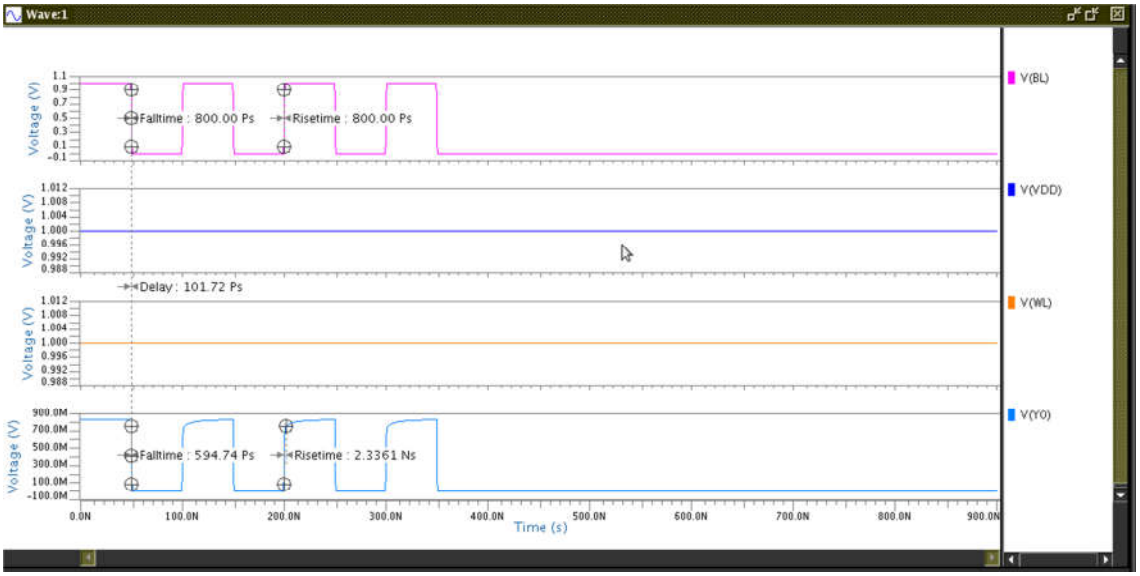

figure8:simulation waveform

Result analysis:

The different parameters like Rise time, fall time, Delay, Power dissipation are calculated from the simulation waveform.

s.no	Parameters	Value
1	Rise time	233.61ps
2	Fall time	594.74ps
3	Delay	101.72ps
4	Power dissipation	1.0605N watts

Comparison table for 6T, 4T, 2T and proposed 2T:

s.no	parameters	6T	4T	2T	Proposed 2T
1	Rise time	800.00ps	705.82ps	307.65ps	233.61ps
2	Fall time	239.11ps	685.63ps	508.87ps	594.74ps
3	Delay	998.53ps	221.23ps	999.16ps	101.72ps
4	Power dissipation	1.2441N watts	2.7964N watts	2.0009N watts	1.0605N watts

APPLICATIONS:

- Embedded use
- Computers
- Hobbyists

CONCLUSION:

In this paper, the area efficiency of proposed SRAM memory cells i.e., the cell constructed with 2 transistors was presented. The parameters like rise time, fall time, delay, power dissipation are greatly enhanced when compared to the existing designs. The area efficiency parameter is achieved by reducing the transistor count .These are designed and implemented in a 130nm technology.

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