CMOS Image Sensor With 3-Stage Cyclic-Cyclic-SAR ADC

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ABSTRACT *In this paper, we provide a theoretical framework for a 1.1-µm-pitch 33-Mpixel 240-fps backside-illuminated 3-D-stacked CMOS image sensor with three-stage cyclic-cyclic-successive-approximation-register (SAR) analog-to-digital converters (ADCs) is devel-oped. The narrow-pitch interconnection technology that connects the pixels and arrayed ADCs inside the pixel area is described. The 3-D-stacked architecture, constructed using the interconnection technology, makes it possible to place a 1932 (H) × 4 (V) correlated-double-sampling/ADC array underneath the pixel area. Furthermore, the pipelined and parallel operation of the three-stage cyclic-cyclic-SAR ADC architecture effectively reduces the conversion time period and power consumption and achieves 12-b pre-cision within one horizontal scan time of 0.92 µs. As a result, the interconnection technology and ADC architecture achieved a high frame rate of 240 fps in 33 Mpixels. Random noise of 3.6 e^- and low power consumption of 3.0 W were attained at an extremely high pixel rate of 7.96 Gpixel/s. A good figure of merit is achieved compared with recently developed image sensors.*

Index Terms— 240 fps, 33 Mpixels, 3-D-stacked, 8K Super Hi-Vision (SHV), cyclic-cyclic-successive-approximation-register (SAR) analog-to-digital converter (ADC), intercon-nections.

Introduction

There is an increasing demand for high-reality video systems. The research and development of 8K Super Hi-Vision (SHV) systems has been promoted for next-generation ultrahigh definition TV (UHDTV) broadcasting systems [1] to convey to viewers a sense of presence and reality. The International Telecommunication Union Radiocommunication Sector has standardized video parameters for UHDTV [2]. The full-specification video signal is required to have a 7680 *(*H*)* × 4320 *(*V*)* pixel count, 120-Hz frame frequency with progressive scanning, wide color gamut, and 12-b tone reproduction.

A 33-Mpixel 120-fps CMOS image sensor with 12-b column-parallel two-stage cyclic analog-to-digital convert-ers (ADCs) has been reported [3]. A two-stage pipelined operation of the first 4-b and second 8-b cyclic ADCs is applied to this CMOS image sensor. Its high efficiency for high-speed low-power operation was demonstrated. An 8K SHV prototype camera with three CMOS sensors of the 1.7-in optical format was also developed [4] for capturing full-specification SHV images. However, the weight of the prototype camera head with three sensors is 45 kg because the camera requires a large-format color-separation prism.

The goal of this paper is to reduce the optical format to two thirds to develop a small 8K SHV camera head. In addition to standard operation of 8K SHV, a high frame rate of 240 fps is required for high-speed video capture. Small-size pixels achieve a deep depth of field, and high sensitivity for small pixels is required.

Recent technology trends in CMOS image sensors have been addressing backside-illuminated (BSI) 3-D-stacked CMOS image sensors [5] because high sensitivity for small pixels with advanced functionality can be achieved in a compact chip size. In these image sensors, a BSI pixel wafer and an application-specific integrated-circuit (ASIC) wafer are stacked with peripheral connection. However, these BSI 3-D-stacked structures are still insufficient for the high frame rate of 8K SHV image sensors. The challenge to increasing the frame rate in this paper is the BSI 3-D-stacked CMOS image sensor using interconnection technology inside the pixel area.

In this paper, we introduced a 1.1-μm 33-Mpixel 240-fps BSI 3-D-stacked CMOS image sensor with three stage cyclic-cyclic-successive-approximation-register (SAR) ADCs. The interconnection technology connects the pixels and arrayed ADCs inside the pixel area and this greatly reduces the response speed of the pixel signal readout. The pipelined operation of the cyclic-cyclic-SAR ADC architecture effectively reduces the conversion time period to 0.92 μs. The interconnection technology and ADC architecture achieve a high frame rate of 240 fps in 33 Mpixels. Random noise of 3.6 e^- and sensor power consumption of 3.0 W are attained at an extremely high pixel rate of 7.96 Gpixel/s.

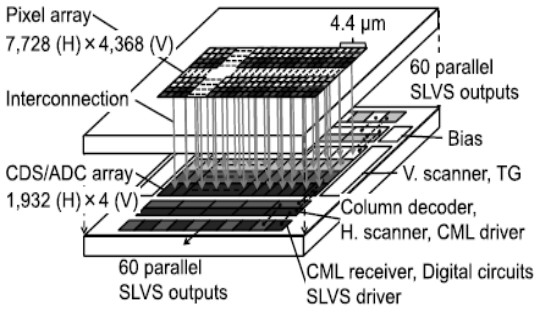


Fig. 1. Structure of BSI 3-D-stacked CMOS image sensor

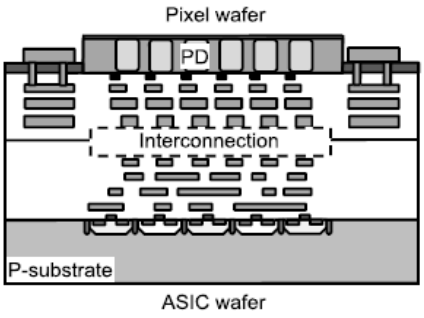


Fig. 2. Cross section of interconnection structure

II.SENSOR ARCHITECTURE

A. Sensor Structure

A 3-D illustration of the BSI 3-D-stacked CMOS image sensor is shown in Fig. 1. The BSI 3-D-stacked structure is fabricated with 4.4-μm-pitch interconnection technology. The effective pixel array is 7728 *(*H*)* × 4368 *(*V*)* with 1.1-μm-pitch 2 × 2-shared pixels on the pixel wafer. Optical black pixels are placed around the effective pixel array, and there are no pixels around the optical black pixels. The ASIC wafer of the chip has a 1932 *(*H*)* × 4 *(*V*)* correlated-double-sampling (CDS)/ADC array composed of a current source load (CSL), CDS with an analog gain amplifier of up to 4.0, and the 12-b three-stage cyclic-cyclic-SAR ADC. There are a total of 20 blocks of column decoders, horizontal scanners, current-mode logic (CML) circuits, digital processing circuits, and scalable low-voltage signaling (SLVS) drivers. The CML circuits are used to suppress interference from logic circuits. Ten blocks are located on the top and the other ten blocks are located at the bottom of the CDS/ADC array. The middle 12 blocks have 480 active columns, and the remaining four right and four left side blocks have 270 active columns. The output codes from the first and second cyclic ADCs and the third SAR ADC are combined into 12-b binary (B) data, and the parallel 12-b data are converted to serial data in the digital processing circuits. Each block has sixfold parallel 1.2-Gb/s SLVS output ports for a total of 120 ports, allowing an aggregate data rate of 96 Gb/s.

B. Interconnection

A cross section of the interconnection structure is shown in Fig. 2. The pixel and ASIC wafers are stacked face-to-face. Both wafers are internally connected inside the pixel area without through-silicon-via, and the metal and insulator layers on both wafers are connected, respectively. The process of fabricating the pixel wafer is optimized for low random noise. Conversely, that of the ASIC wafer is optimized for high-speed operation of the readout circuits.

A block diagram of the pixels, ADCs, and interconnec-tions in a column is shown in Fig. 3. On the pixel wafer, 4*(*H*)* × 4368 *(*V*)* pixels are placed in the column. A 4 × 4-pixel unit consists of four sets of 2 × 2-shared pixels. The 4 × 4-pixel unit repeats along the column in the pixel wafer. Four CDS/ADCs are placed in the column of the ASIC wafer. A CDS/ADC unit is composed of a CSL, CDS, and the three-stage cyclic-cyclic-SAR ADC. The pixels and CDS/ADCs are overlaid in the column. Each set of four 2 × 2-shared pixels shares output lines and connects with the four CDS/ADCs by the interconnections in the column. The horizontal pitch of the CDS/ADCs and the

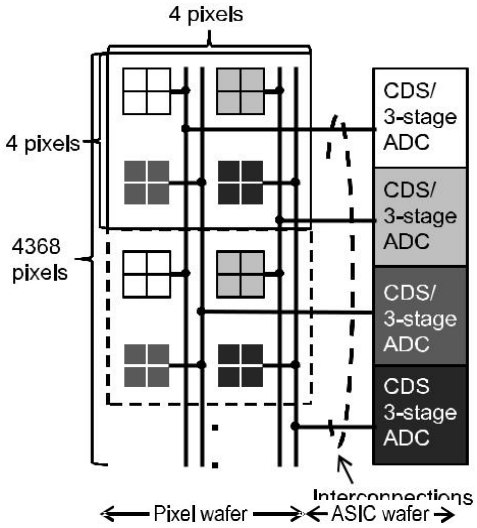


Fig. 3. Block diagram of pixels, ADCs, and interconnections in column.

interconnections is selected to be 4.4 μm, which is determined by considering the ADC architecture and the size of the 2 × 2-shared pixels. In total, 1932 columns and 7728 pixels are placed horizontally.

C. 12-b 3-Stage Cyclic-Cyclic-SAR ADC

Architecture: A cyclic ADC is suitable for high-speed high-resolution column-parallel ADC architecture for CMOS image sensors [6]. To achieve a more efficient design required for 33-Mpixel 120-fps image sensors, pipelined two-stage operation of two cyclic ADCs is proposed and its power-efficient design is demonstrated [3], [11]. To meet the aggres-sive specifications of the 33-Mpixel 240-fps image sensor, a pipelined three-stage operation using two cyclic ADCs for the first and second stages and an SAR ADC for the third stage is introduced.

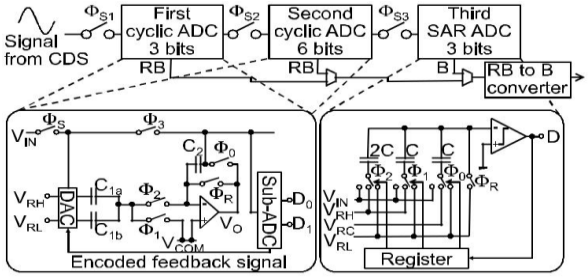


Fig. 4. Architecture of 12-b cyclic-cyclic-SAR ADC.

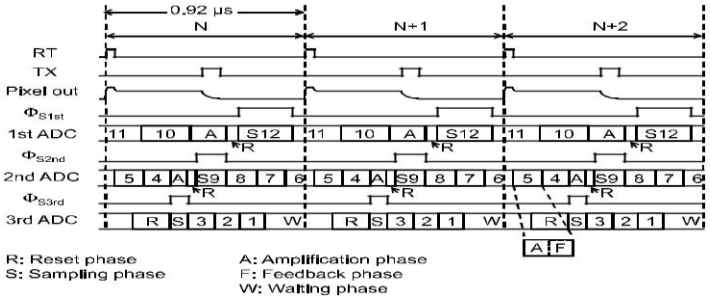


Fig. 5. Simplified timing diagram illustrating pipelined operation.

The architecture of the implemented 12-b three stage cyclic-cyclic-SAR ADC is shown in Fig. 4. This three-stage ADC is composed of a first cyclic ADC, which converts the upper 3 b, a second cyclic ADC, which converts the middle 6 b, and a third SAR ADC, which converts the lower 3 b. The three-stage pipelined operation relaxes the power budget of the cyclic ADCs which use a power-hungry operational amplifier. The cyclic ADC has a capability of residue amplification with a gain of two per every cycle and this relaxes the analog precision of latter stages. The SAR ADC stage requires only 3-b precision and can use very small-size capacitors thanks to the residue amplification with the total gain of 2^9 of the former two cyclic ADC stages. The SAR ADC consumes a small amount of power thanks to the comparator used and therefore the conversion speed of the entire 12-b ADC is increased by the three-stage pipelined operation with compara-ble power consumption to the previous two-stage cyclic ADC architecture. These architectural advantages are fully exploited in the designed column-parallel 12-b ADC.

2) Timing Diagram and Operation: A timing diagram of the three horizontal periods describing the pipelined operation is shown in Fig. 5. One horizontal scanning time is 0.92 μs at a frame rate of 240 fps with 4500 vertical scanning lines. The labels RT and TX represent control signals for the reset transistor and transfer gate in the pixels, respectively.

An analog CDS cancels the reset noise in the pixel output signal. The analog output signal from the CDS circuit is sampled and converted into 12-b digital data in the three-stage cyclic-cyclic-SAR ADC.Each cyclic ADC consists of a single-ended amplifier, two capacitors (C_1 and C_2), a sub-ADC with two comparators and logic circuit, switch transistors, and a digital-to-analog converter with a decoder. Depletion-mode MOS capacitors with low voltage dependence of the capacitance are used for C_1 and C_2, which can suppress differential nonlinearity (DNL) errors [7]. To generate a three-state internal reference, the sam-pling capacitor C_1 is divided into C_{1a} and C_{1b}. The 3-b SAR ADC consists of a capacitor array of 2C, C, and C, a com-parator, switch transistors, and a register and control logic. To reduce the layout area, a capacitor of 4C is eliminated, and a reference voltage of V_{RC} is added to this SAR ADC.

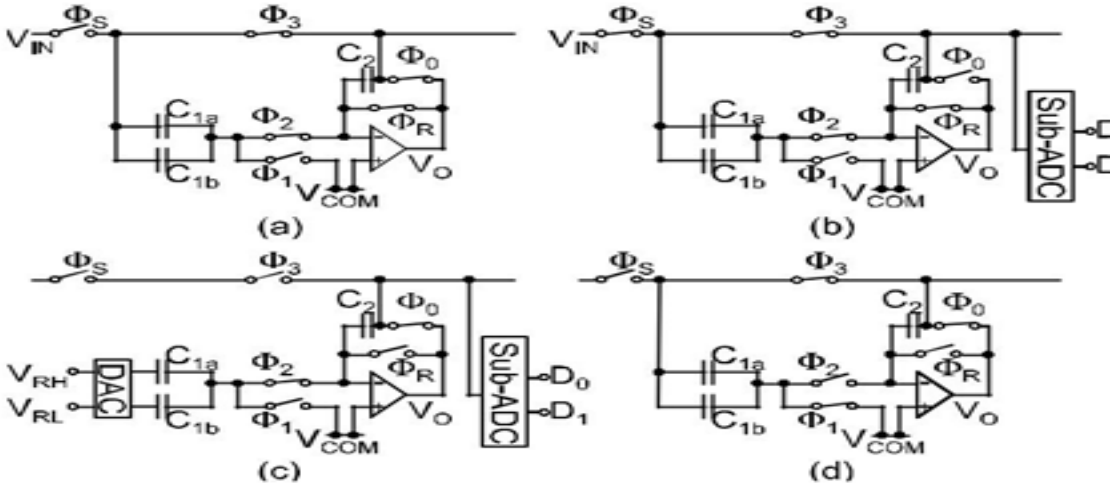


Fig. 6.Phase diagram of cyclic ADC showing circuit connection. (a)reset phase.(b)Sampling phase.(c)Amplification phase.

(d) Feedback phase.

Each cycle of the cyclic ADC consists of [Fig. 6(a)] reset phase, [Fig. 6(b)] sampling phase, [Fig. 6(c)] amplification phase, and [Fig. 6(d)] feedback phase. First, all the capacitors in the cyclic ADC are initialized during the reset phase to remove the residual charge, as shown in Fig. 6(a). Then, the output signal from the CDS circuit is sampled during the signal sampling phase, and the sub-ADC generates a three-state 1.5-b redundant binary (RB) code for the most significant bit (MSB), as shown in Fig. 6(b). The sampled signal is multiplied by a gain of two, and the reference voltage, as determined by the sub-ADC in the signal sampling phase, is subtracted during the amplification phase, as shown in Fig. 6(c). At the end of the amplification phase, the sub-ADC generates a 1.5-b RB code for MSB − 1. Subsequently, the amplified output signal is returned to the input terminal of the ADC during the feedback phase, as shown in Fig. 6(d). The amplification and feedback phases are repeated for two cycles to obtain the first 3-b resolution. During the subsequent amplification phase, the output of the first cyclic ADC is connected to the second cyclic ADC by turning ON the switch $_S$ during the signal sampling phase of the second cyclic ADC, and a sub-ADC of the second cyclic ADC generates three-state 1.5-b RB code, as shown in Fig. 6(b). The amplification and feedback phases are repeated for five cycles to obtain the second 6-b resolution. During the subsequent amplification phase, the output of the second cyclic ADC is connected to the third SAR ADC by turning ON the switch $_{S3}$, as shown in Fig. 4.

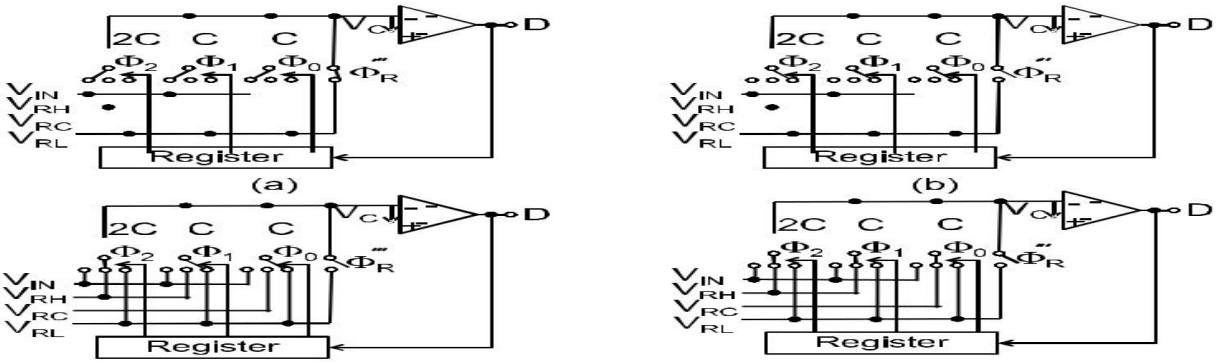


Fig. 7.Phase duiagram for 3-b SAR ADC showing circuit Connection (a)sampling phase (b)Holding phase (c) Redistribution phase for third bit. (d)Redistribution phase fofirst bit.

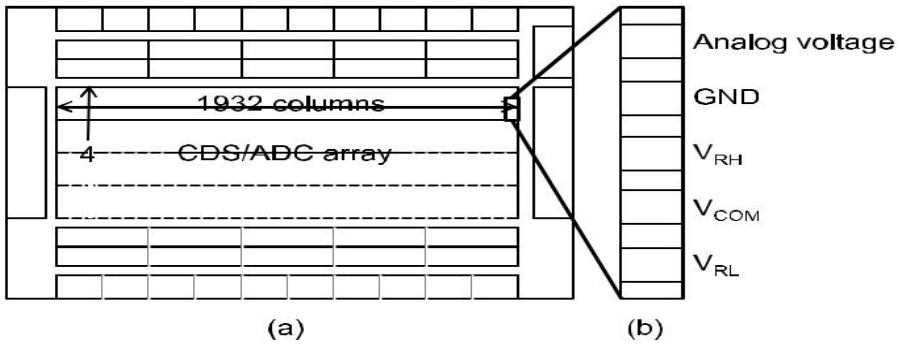


Fig. 8. (a) Schematic layout of ASIC wafer. (b) Schematic layout of metal wiring of first cyclic ADC.

The third 3-b SAR ADC architecture generates 3-b B code, whose phase diagram consists of [Fig. 7(a)] sampling phase, [Fig. 7(b)] holding phase, and [Fig. 7(c) and (d)] redistribution phase. First, a total charge is stored on the capacitors during the sampling phase, as shown in Fig. 7(a). A voltage of $V_C = V_{IN} - 2V_{RL}$ is applied to the comparator input during the holding phase, as shown in Fig. 7(b). The first conversion step for the third bit during the redistribution phase is shown in Fig. 7(c). The capacitor of $2C$ forms a 1:1 capacitance divider with the remaining capacitors. The comparator input voltage V_C becomes $V_C = V_{IN} - V_{RH}/2 - 3V_{RL}/2$. If $V_{IN} > V_{RH}/2 + 3V_{RL}/2$, the comparator output becomes high, result-ing in the third bit being set to 1. On the other hand, if $V_{IN} < V_{RH}/2 + 3V_{RL}/2$, the third bit is set to 0. The second conversion step for the second bit is performed in the same sequence. The third conversion step for the first bit is by the capacitor of C and the reference voltage of V_{RC} instead of V_{RH}, as shown in Fig. 7(d). Here, $V_{RC} = (V_{RH} + V_{RL})/2$.

As a result of the three-stage ADC architecture, while the third SAR ADC performs the 3-b conversion of the Nth row, the second cyclic ADC converts the 6-b signal of the $(N+1)$th row, and the first cyclic ADC converts the 3-b signal of the $(N + 2)$th row, which means that the three ADCs work in a pipelined fashion. The three-stage pipelined operation effectively reduces the conversion time period to 0.92 μs.

Layout Area: The schematic layouts of the ASIC wafer and the first cyclic ADC on the wafer are shown in Fig. 8(a) and (b), respectively. A 3-D-stacked interconnection technology enables the placement of arrayed CDS/ADCs. The number of vertically placed CDS/ADCs is four and that of horizontally placed CDS/ADCs is 1932. Thus, the number of horizontally placed CDS/ADCs, which are connected to the same wiring, is half that of the previous 8K image sensor. Current is consumed in an amplifier and comparators of the first and second cyclic ADCs, and voltage drops in the power supply wiring of the cyclic ADCs. The voltage drop of the center first and second cyclic ADCs is set to 0.1 V, which is the same as that of the previous sensor. We can then narrow the power supply wiring of the cyclic ADCs. As a result, the layout area of the cyclic ADCs is reduced.

The architecture of the third 3-b SAR ADC is shown on the right in Fig. 4. A conventional 3-b SAR ADC requires capacitor layout areas of *C*, *C*, 2*C*, and 4*C*, for successive approximation operation. In this 3-b SAR ADC, the capacitor layout area of 4*C* is eliminated by adding a reference voltage V_{RC} .

The layout area of the three-stage cyclic-cyclic-SAR ADC is reduced by narrowing the power supply wiring in the first and second cyclic ADCs and eliminating the capacitor of 4*C* in the third SAR ADC.

4) Power Consumption: By exploiting the amplifier function of the cyclic ADCs, the power consumption of the previous two-stage cyclic ADC was decreased by reducing the size of the sampling capacitor of the second cyclic ADC when the bit allocations of the first and second cyclic ADCs were 4 and 8 b, respectively [3]. In the three-stage cyclic-cyclic-SAR ADC, the bit allocations of the first and second ADCs are set to 3 and 6 b. Thus, 12 and 9-b accuracy are required for the first and second ADCs, respectively. Amplifier gains of more than 84 and 66 dB are required for the first and second ADCs when the input-referred error is assumed to be 1/4 of the least significant bit (LSB). The results of a dc simulation using SPICE indicate that peak gains of the amplifier are 85 and 84.4 dB for the first and second ADCs. The SPICE simulation was carried out across all process-voltage-temperature corners to determine the minimum dc gain. Therefore, the requirements for the gains are acceptable.

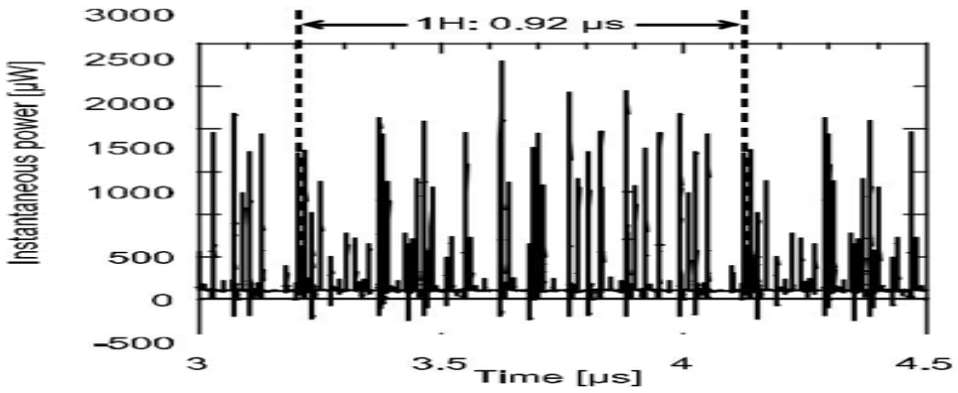


Fig. 9. Simulated instantaneous power of 12-b cyclic-cyclic-SAR ADC

The results of a transient simulation using SPICE are shown in Fig. 9, which is the instantaneous power of the cyclic-cyclic-SAR ADC during one horizontal scan time. Integration of instantaneous power during one second shows that the power consumption of the cyclic-cyclic-SAR ADC is 120 μW. The power consumption caused by the dc current of the amplifier and comparators in the first and second cyclic ADCs and the comparator in the third SAR ADC is 105 μW. This accounts for 87.5% of the total power consumption of the ADC.

Power consumption is suppressed to 120 μW by low power-consumption operation of the first and second cyclic ADCs and by placing the SAR ADC as the third stage in spite of the double operation speed.

5) 12-b Accuracy: The first and second cyclic ADCs output a 1.5-b RB code, which is expressed with two decision levels for each cycle. The use of RB codes reduces the precision requirements of the comparators. The RB codes from the first and second cyclic ADCs overlap the next stage to generate 12-b B code in the RB-to-B converter.

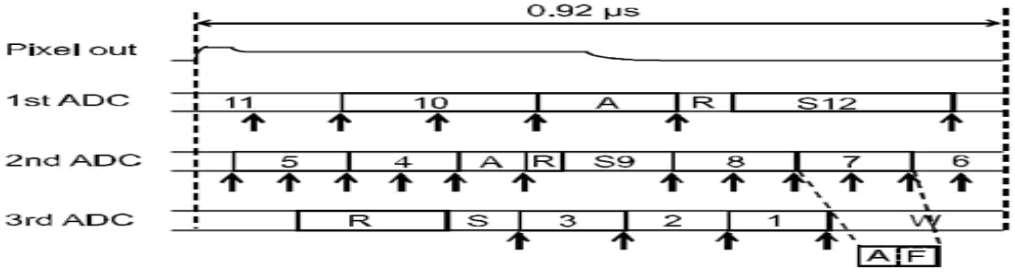


Fig. 10. Latch timing of 12-b signal during one horizontal period

A latch timing of a 12-b signal during one horizontal period is shown in Fig. 10. The latch timings are indicated with arrows, which show the end of the sampling phases, amplification phases and feedback phases. All latch timings are designed not to overlap each other when the bit allocations are 3, 6, and 3 for each stage. High accuracy is attained by preventing analog interference from the clock timing. We considered bit allocations of 3, 6, and 3 and 3, 5, and 4 for each three-stage ADC. Bit allocations of 3, 6, and 3 were better than those of 3, 5, and 4 from the viewpoint of preventing overlap of latch timings.

The settling times of the amplifier in the first and second cyclic ADCs are calculated from transient analysis using SPICE simulation. All settling errors are designed within 1 LSB of 12-b accuracy in all operation phases.

The three-stage cyclic-cyclic-SAR ADC is designed to obtain 12-b accuracy for these reasons.

6)Comparison of the Designed ADC: Table I compares the design of the ADC used in the 33-Mpixel image sensor of this work with that of the previous two-stage cyclic ADCs. The conversion time period is halved because of the pipelined operation of the three-stage cyclic-cyclic-SAR ADC.The layout area is less than half that of the previously designed two-stage cyclic ADC because of narrowing the power supply wiring in the cyclic ADCs and eliminating the capacitor of 4*C* in the third SAR ADC. The power consumption is almost the same, while the conversion time period is halved because of the high efficiency for low-power operation in the cyclic ADCs and using an SAR ADC as the third stage.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Fabrication and Implementation

A prototype image sensor has been fabricated using 3-D interconnection process technology with 45-nm 1-polysilicon 4-metal process for the pixel wafer and 65-nm 1-polysilicon 5-metal process for the ASIC wafer. A micrograph of the monochrome image sensor die is shown in Fig. 11. The viewed side is the backside of the pixel wafer of the BSI 3-D-stacked CMOS image sensor. The die size is 14 mm*(*H*)* × 10 mm*(*V*)*, which fits into one shot reticle. There are pads of SLVS outputs, supply voltages of the phase locked loop, and digital supply voltages on the top and bottom of the die. There are pads of digital inputs, reference voltages, voltages for pixels, and analog supply voltages on the left and right of the die.

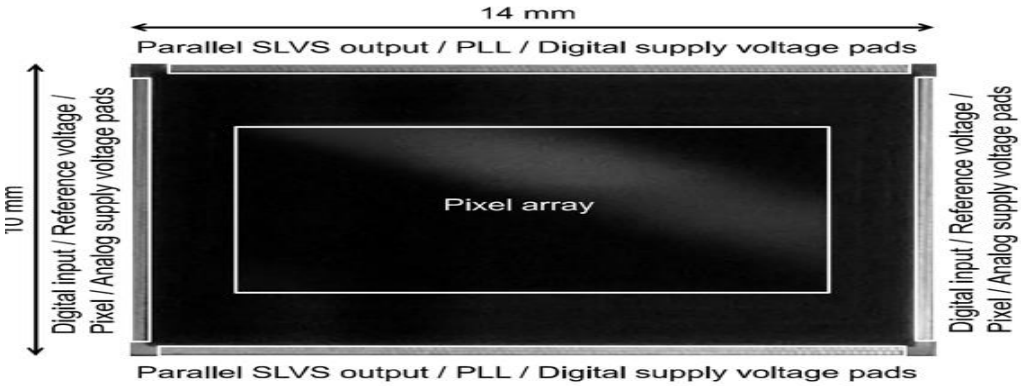


Fig. 11. Die micrograph of image sensor.

The monochrome sensor was used for all measurements. The measurement system consists of a measurement camera head and signal processor. Raw data are directly output from the field-programmable gate array to the logic analyzer for measurement.

B. Captured Image

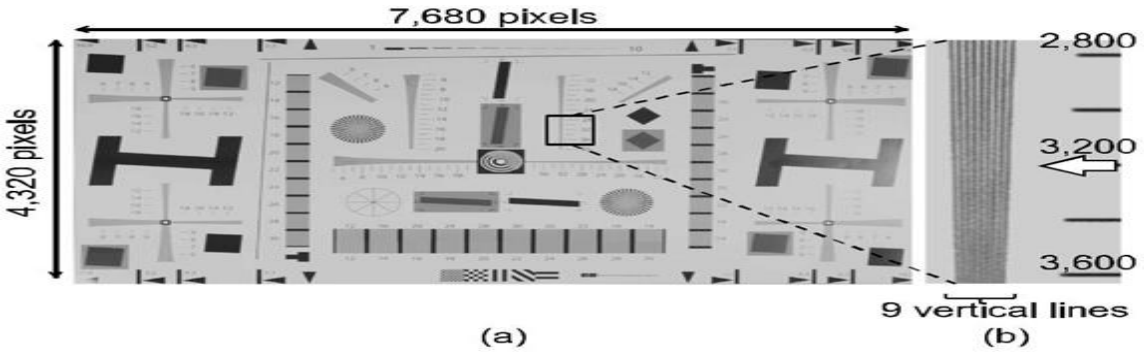
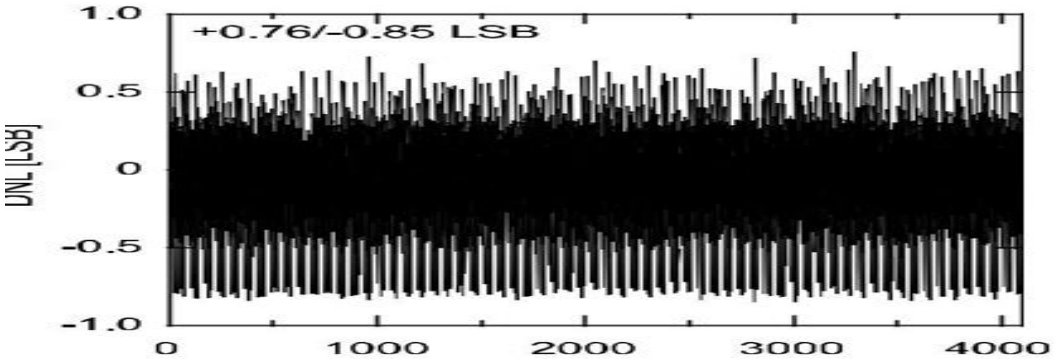


Fig. 12. (a) Reproduced full-size image. (b) Magnified portion of wedge shape.

A reproduced full-size image taken at 240 fps with the image sensor is shown in Fig. 12(a). Vertical fixed pattern noise is canceled with the signal processor by using black reference rows. The linearity of pixel output is good for signal levels from dark to saturation. Image capturing correc-tions, such as gamma, knee, and white clip, are turned OFF. The color temperature of the light is 5600 K. In the image, no deadline errors are detected. This means that the interconnec-tion structure is fully connected. A magnified portion of the wedge shape is shown in Fig. 12(b). This image indicates that a resolution of more than 3200 TV lines is confirmed when the *f* -number of the lens is set to 4.0. When incident light with a saturation signal is irradiated, the image lag level after one frame is less than the random noise level.

B Performance of the Fabricated Cyclic-Cyclic-SAR ADC



C

D

Fig. 13. Measured DNL at 240 fps.

The measured DNL of the implemented 12-b three stage cyclic-cyclic-SAR ADC driven at 240 fps is shown in Fig. 13. The DNL is within +0.76 to −0.85 LSB, which indicates that there is no missing code. This graph is of raw data without calibration when a sine wave is input to the ADC. Many ADCs from each of the 20 blocks are measured at random and all measured DNL are within 1 LSB. As a result, 12-b accuracy is obtained.

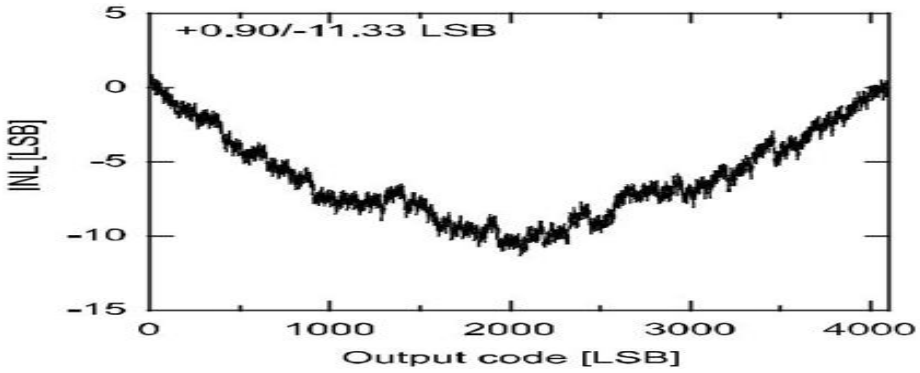


Fig. 14. Measured INL at 240 fps.

The measured integral nonlinearity (INL) is shown in Fig. 14. The INL is within +0.90 to −11.33 LSB, which indicates that the variation is within 0.30% of the 12-b signal range. The INL shows a negative value because the voltage dependence of the MOS capacitors of C_{1a} , C_{1b}, and C_2 in the cyclic ADC appeared in it. Analysis is shown in [7] in detail.

D. Specifications

The supply voltages are 1.2/2.5 V for digital and 33 Mpixels and the pixel size is 1.1 μm. The maximum frame rate of 240 fps is achieved because of the con-version time period of 0.92 μs. The ADC resolution is 12 b. The measured DNL is within +0.76 to −0.85 LSB and the INL is within +0.90 to −11.33 LSB. 12-b accuracy is attained in the implemented cyclic-cyclic-SAR ADC. The conversion gain of 92 μV/e^- is obtained, which is calculated from the cross point of the sensor output signal and photon shot noise. The gain of the source follower amplifier is included in the value of the conversion gain. The sensitivity of 0.55 V/lux·s is obtained without a micro lens and color filter. A Commission Internationale de l'Éclairage (CIE) A-light source is used and an infrared cut filter is attached at the time of measurement. A full-well capacity of 5700 e^- is obtained from the signal when the noise begins to decrease in the graph of the sensor output signal and photon shot noise. When incident light with half saturation signal is irradiated, the photo response nonuniformity is less than 1.3%.

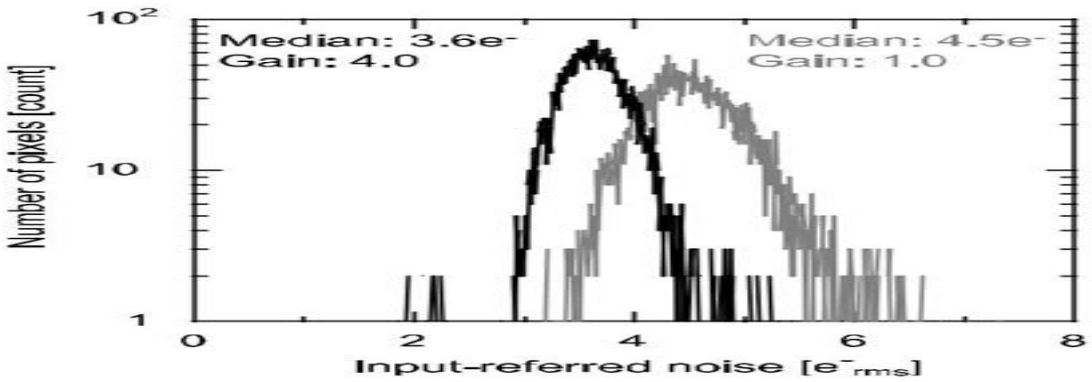


Fig. 15. Measured random noise.

The noise histogram for 4560 pixels is shown in Fig. 15. The median of the histogram indicates that random noise is 4.5 e^-_{rms} at an analog gain of 1.0. The input-referred random noise is 3.6 e^-_{rms} at an analog gain of 4.0. Measurements are conducted at room temperature and under the dark condition. These random noises are obtained while attaining an extremely high pixel rate of 7.98 Gpixel/s.

The breakdown of the sensor power consumption is shown in Table III. A total power consumption of 3.0 W is measured at a pixel rate of 7.98 Gpixel/s under the dark condition. It is composed of the power consumed by analog circuits, digital circuits, and pixels. The power consumption of the analog
circuits is from the CSL, CDS, and three-stage cyclic-cyclic-SAR ADC, that of the digital circuits is from the CML receiver and SLVS driver and that of pixels is from the drain voltage of the source follower and reset transistor.

E. Performance Comparison

The pixel rate f_p is defined as (number of pixels × frame rate). The FoM_1 is defined as (power×noise×10^9) over (pixel rate) and means the noise and power performance per pixel rate. The FoM_2 is defined as (power × noise × gain × 10^{12}) over (pixel rate × 2^b) and means power performance per dynamic range and pixel rate. These FoMs of the fabricated image sensor are used in the performance comparison.

An FoM_1 of 1.36 e^- · nJ and an FoM_2 of 1.32 e^- · pJ/step are obtained with our sensor in [12] and this paper. Smaller FoM values are better. The FoMs of our image sensor are comparable or better than those of the others. These

results show that low noise and low power consumption are achieved while an extremely high pixel rate of 7.96 Gpixel/s is attained.

IV. SUMMARY

The 1.1-μm 33-Mpixel 240-fps BSI 3-D-stacked CMOS image sensor with 12-b three-stage cyclic-cyclic-SAR ADCs. The ADC architecture and the interconnection technology achieve a high frame rate of 240 fps in 33 Mpixels for the first time. Random noise of 3.6 e^- and low power consumption of 3.0 W are attained at an extremely high pixel rate of 7.96 Gpixel/s.

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