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Design of New Double-Tail Comparator with Low-Voltage Low-Power and Area Efficient

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Abstract

High speed dynamic regenerative comparators are used in low power and area efficient analog to digital converters to improve speed and power efficiency. Speed and power consumption are the two factors that define the comparators accuracy. A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. In this paper, a new double tail comparator is proposed by modifying the low voltage low power double tail comparator circuit for power efficient and high speed operation. In the proposed dynamic double tail comparator System both the power dissipation and delay time would be significantly reduced. The simulations are carried out in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology. From this it is evident that with the proposed comparator design there is 55.5% in delay and 35.5% reduction in power dissipation

Keywords: double tail comparator, High speed analog to digital converters.

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most of the analog-to-digital converters (ADCs). Many of the high-speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra deep sub-micrometer (UDSM) CMOS technologies suffer from very low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [2]. Hence, designing of high-speed comparators is more challenging when supply voltage is smaller. In other words, in this technology, to achieve high speed, larger transistors are required to compensate the reduction of the supply voltage, which also means the more die area and power is needed. Besides, low-voltage operation results in the limited common-mode input range, which is important in high-speed ADC architectures, such as flash ADCs.

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison. Vp is the input voltage (pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator.

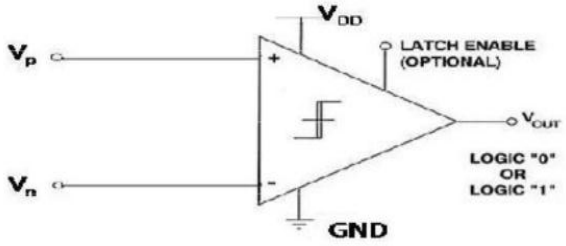


Figure: Schematic of Comparator

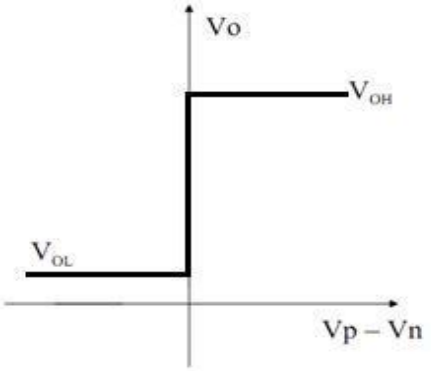


Figure: Ideal voltage transfer characteristic of comparator

II. BLOCK DIAGRAM OF COMPARATOR

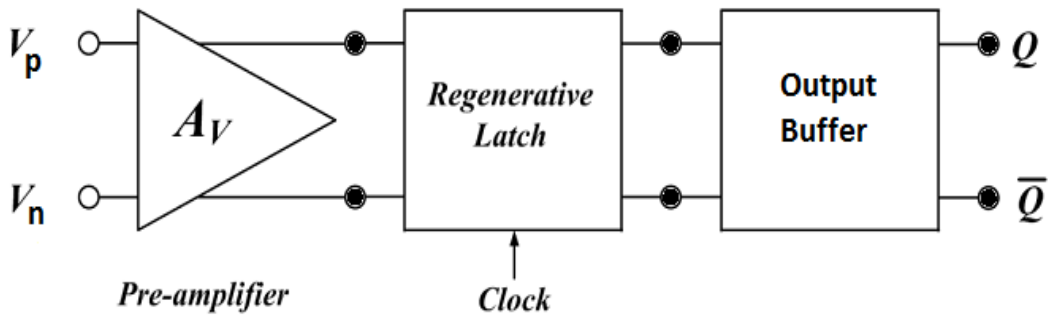


Figure: Block diagram of Comparator

A clocked comparator generally consists of two stages. The first stage is to interface the two input signals. The second stage (regenerative stage) consists of two cross coupled inverters, where each input is connected to the output of the other one. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched by either NMOS or PMOS transistor [3]. In many applications comparator speed, power dissipation and transistor count are more important. If comparator speed is a priority, the regenerative stage could be designed to start its operation from the midway between power supply and ground. For example, in conventional comparator however, the static power consumption reduction, hence transistor count increases there by reducing the speed.

III. REVIEW OF EXISTING COMPARATORS

A. Conventional Dynamic Comparator

The schematic circuit of Conventional dynamic comparator is shown in fig.1. The operation of the conventional dynamic comparator is as follows: During pre- charge phase (CLK = 0) and Mtail transistor will be off, the transistors M7 and M8 will pull both the Outn, Outp (output nodes) to VDD in order to define a start condition and to have a valid logical level during reset [1].

During evaluation phase (when CLK = VDD) transistors M7, M8 are off and corresponding Mtail transistor will be on. Output nodes (Outp, Outn) which had been pre-charged to VDD, start to discharge at different discharging rates depending on the input voltages (VINP and VINN).Assuming the case where VINP > VINN, the output node Outp start to discharge at a faster rate than Outn, hence Outp (discharged by transistor M2 drain current), falls down to 'VDD–|Vthp|' before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on to initiate the latch regeneration with the help of two back-to-back inverters (M3-M5 and M4-M6). Thus, the output node Outn will be pulled to VDD and Outp discharges to ground. If the input voltage VINP is less than VINN, the circuit works vice versa [3].

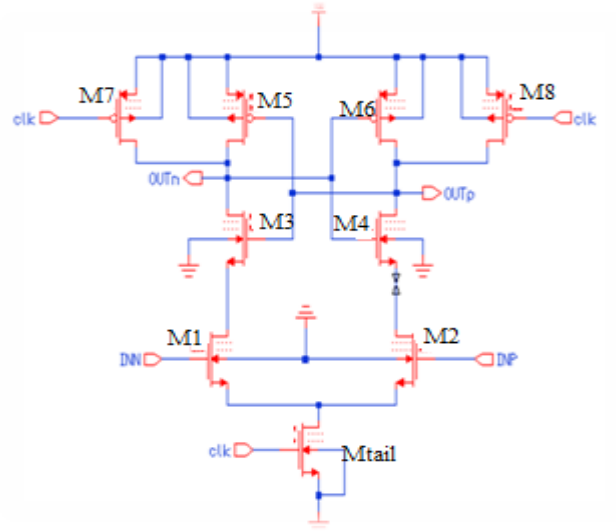


Figure 1: Schematic Circuit of Conventional dynamic comparator

The main advantage of Conventional dynamic comparators are high input impedance, rail-to-rail output swing, and no static power consumption.

B. Conventional Double Tail Comparator:

The schematic circuit of Conventional double tail comparator is shown in fig.2. The operation of the conventional double tail comparator is as follows: During pre-charge phase (CLK = 0), Mtail1 and Mtail2 transistors will be off while corresponding M3 and M4 transistors pre-charge the nodes fn and fp to VDD, which in turn make MR1 and MR2 transistors to discharge the output nodes Outn and Outp to ground [1].

During decision-making phase (CLK = VDD) Mtail1 and Mtail2 transistors will turn on, then the corresponding transistors M3 and M4 turn off and the voltages at nodes fn, fp start to drop [4]. The intermediate stage formed by these transistors MR1 and MR2 passes ΔVfn(p) towards the cross

coupled inverters and provides a good shielding between the input and output to reduce the value of kickback noise.

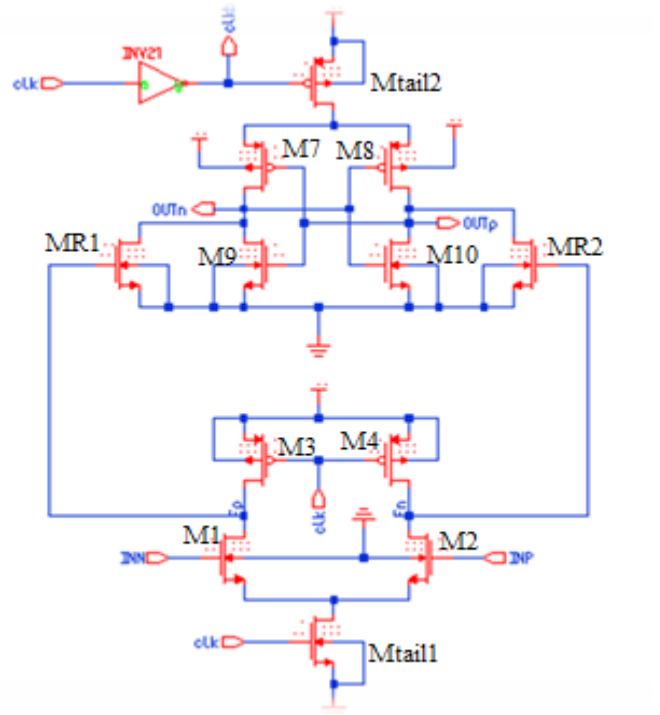


Figure 2: Schematic circuit of Conventional double tail dynamic comparator

The main advantage of conventional double-tail comparator is less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator.

C. Modified Double-Tail Dynamic Comparator (Main Idea):

The schematic circuit of Modified double tail dynamic comparator (Main Idea) is shown in fig.3. The operation of the comparator is as follows: During pre-charge phase(CLK = 0), Mtail1 and Mtail2 are off, avoiding static power, M3 and M4 pulls both outn and outp (output nodes) to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground [6].

During evaluation phase (CLK = VDD), Mtail1, and Mtail2 are on, transistors M3 and M4 turn off, from the beginning of this phase, the control transistors are still off (since outn and outp are about VDD) [5].Thus, outn and outp start to drop with different rates according to the input voltages(VINP and VINN).

Assuming the case VINP > VINN, thus outn drops faster than outp, (since M2 provides more current than M1). As long as outn continues falling, the corresponding pMOS control transistor (M_{c1}) starts to turn on, pulling outp node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing outn to be discharged completely. Despite the effectiveness of the main idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., M_{c1}, M 1, and M_{tail1}), resulting in static power consumption. Modified double tail comparator has a better performance than double-tail architecture in low-voltage applications.

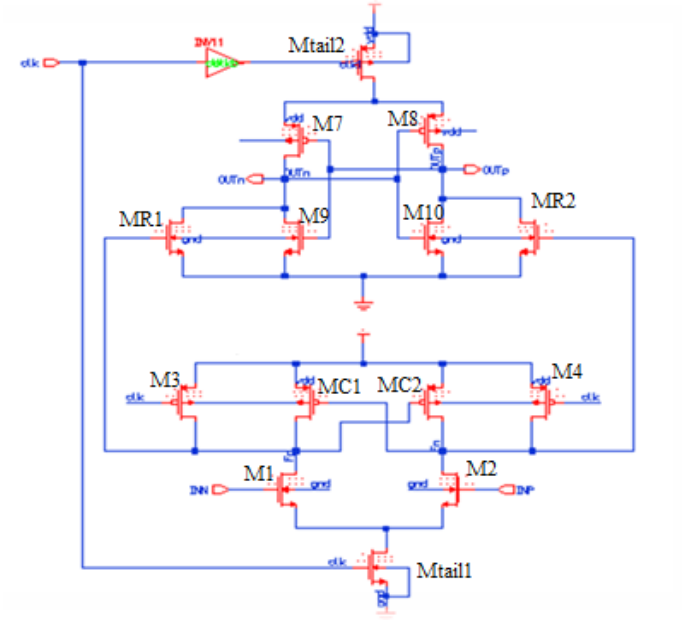


Figure 3: Schematic Circuit of Modified Double Tail Comparator a) Main Idea

D. Modified Double-Tail Dynamic Comparator (Final Structure):

The schematic circuit of Modified double-tail dynamic comparator (Final Structure) is shown in fig.4. In order to overcome the problem in modified double tail dynamic comparator two n-MOS switches are used below the input transistors [M_{sw1} and M_{sw2}]. The operation of the modified double tail comparator is as follows. During pre-charge phase (CLK = 0, Mtail1 and Mtail2 transistors are off, avoiding static power), M3 and M4will pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground [7].

During evaluation phase (CLK = VDD, Mtail1, andMtail2 transistors are on), transistors M3 and M4 are off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD) [10]. Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP >VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, PMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD, so another control transistor (Mc2) will off, allowing fn to be discharged completely [8].

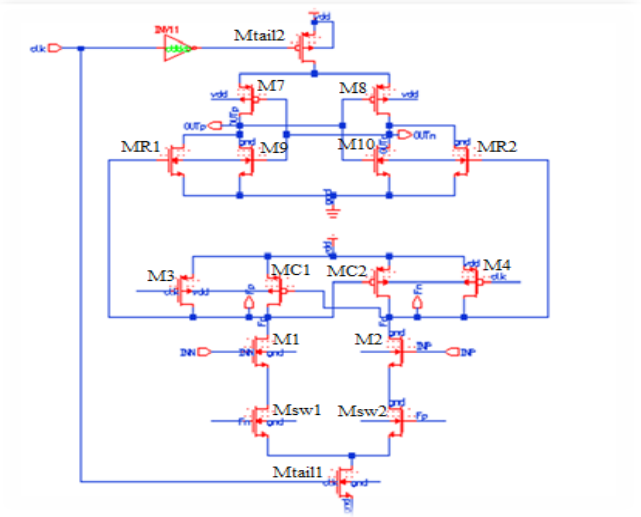


Figure 4: Schematic Circuit of Modified Double Tail Comparator b) Final Structure

IV. PROPOSED COMPARATOR

The schematic circuit of proposed comparator is as shown in fig 5.The operation of the circuit is as follows: During pre-charge(reset) phase clk=0, both M9 and M10 pmos transistors are turned on and they pull fp and fn node capacitances to VDD, which turns on both M5 and M8 nmos transistors and make fp and fn nodes to discharge to ground. Sequentially pmos transistors M1, M2 turn off and they make outp and outn nodes to be discharged to ground.

During evaluation (decision) phase clk=VDD, fp and fn node capacitances are discharged from VDD to ground in a different time rate proportion to the magnitude of each input voltage [9]. As a result, an input dependent differential voltage is formed between fp and fn nodes. Once either fp or fn node voltage drops down below a value small enough to turn off M5/M8 the corresponding output nodes will be charged to VDD. If Vinp>Vinn the outp will be high and it is low otherwise.

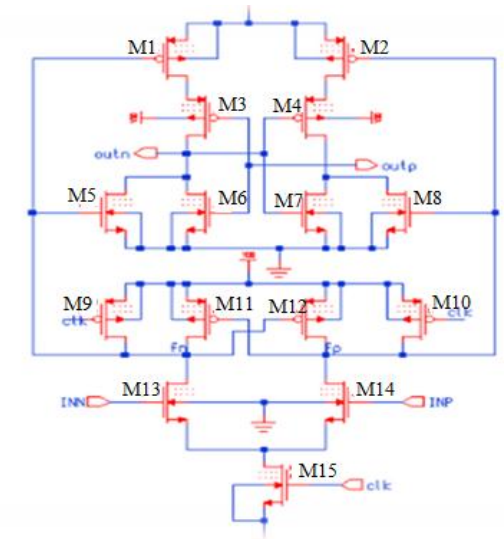


Figure 5: Schematic circuit of Proposed comparator

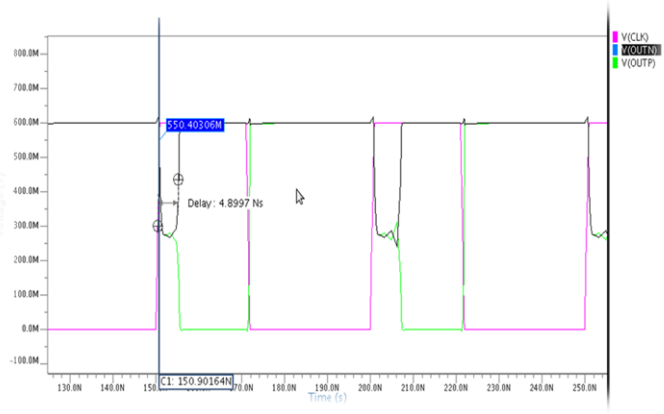


Figure 6: simulation waveform

V.SIMULATION RESULTS AND PERFORMANCE COMPARISONS

All the comparators were designed using Chartered Semiconductor Limited's 0.13µm CMOS process technology, at a supply voltage of 0.6V and 0.8V, using MENTOR TOOLS. The performance of the proposed comparator is evaluated and compared with existing comparators. Table I summarize the performance of the reviewed existing comparators and proposed designs.

SNO	Rise Time 0.6v 0.8v	Fall Time 0.6v 0.8v	Delay 0.6v 0.8v	Power dissipation 0.6v 0.8v	No. of transistors used
Conventional dynamic comparator	800.00ps 307.08ps	4.6343ns 424.94ps	4.8997ns 29.541ns	496.967pw 667.354pw	09
Conventional double tail dynamic comparator	800.00ps 800.00ps	800.00ps 800.00ps	216.15ps 242.26ps	1.5669nw 1.0896nw	12
Modified Double Tail Comparator a) Main Idea	800.00ps 800.00ps	800.00ps 800.00ps	1.5949ns 49.768ns	1.0588nw 1.521nw	14
Modified Double Tail Comparator b)Final Structure	800.00ps 800.00ps	99.301ps 99.301ps	185.54ps 20.503ns	1.0590nw 1.514nw	16
Proposed comparator	800.00ps 800.00ps	429.89ps 800.00ps	429.89ps 424.34ps	540.060ps 735.31ps	15

VI. APPLICATIONS:

Comparators are the key design elements for a wide range of applications such as

- Analog to digital converters.
- Test circuit applications.
- Schmitt trigger.

Flash A/D Converter:

A flash ADC is a type of analog-to-digital converter shown in below fig.7. that uses a linear voltage ladder and a comparator at each ladder to compare the input voltage with that of successive reference voltages. Often these reference ladders are constructed using many resistors. The output of these comparators are generally fed into a digital encoder, which converts these inputs into a binary value. Flash converters are extremely fast compared to other types of ADCs.

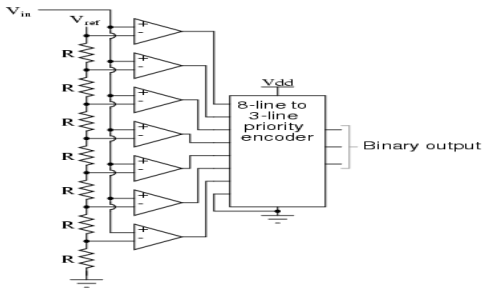
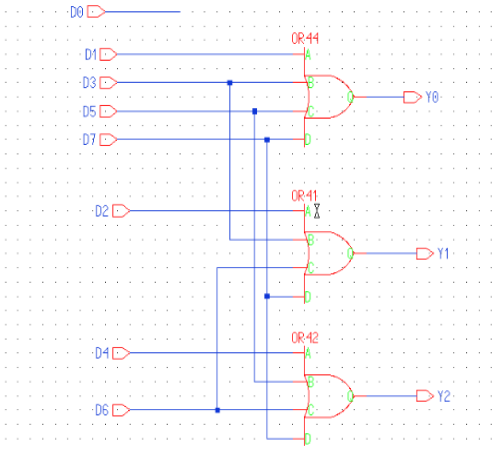


Figure 7: Schematic of 3-Bit Flash ADC



Priority encoder block

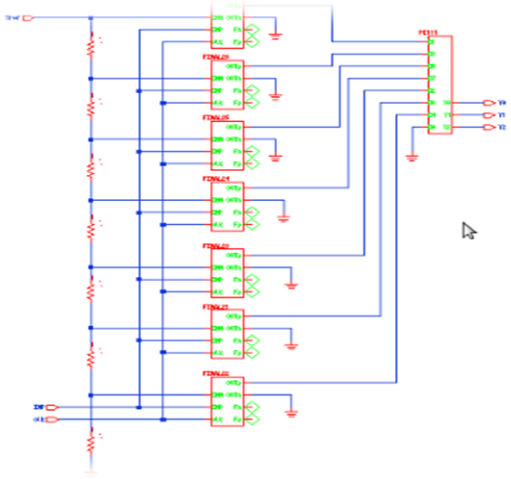


Figure 8: Schematic circuit of 3-Bit Flash ADC with existing comparator

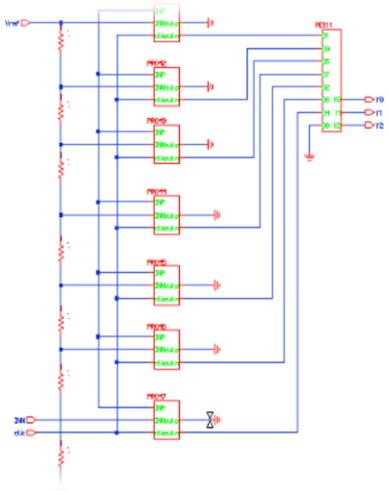


Figure 9: Schematic circuit of 3-Bit Flash ADC with proposed comparator

COMPARISON TABLE-II

Parameters	3- Bit Flash ADC	3- Bit Flash ADC
Rise Time	800.00ps	800.00ps
Fall Time	800.00ps	800.00ps
Delay	48.957Ns	27.752Ns
Power Dissipation	3.571Nw	3.254Nw

VII. CONCLUSION

In this paper, comprehensive delay analysis for clocked dynamic comparators were presented. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Based on double tail structure a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Pre-layout simulation results in 0.13-μm CMOS technology confirmed that the delay and power dissipation of the proposed comparator is reduced to a great extent in comparison with the existing comparators.

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