International Journal of Applied Engineering Research ISSN 0973-4562 Volume 13, Number 9 (2018) pp. 6780-6789

Design of New Dual Edge Triggered Sense Amplifier Flip-Flop with Low Area and Power Efficient

Ms. Sheik Shabeena[1], R.Jyothirmai[2], P.Divya[3], P.Kusuma[4], Ch.chiranjeevi[5]

[1]Assistant Professor, [2,3,4,5]Student

Dadi institute of engineering and technology, Visakhapatnam, Andhra Pradesh-531002, India.

ABSTRACT

A new dual edge trigged sense-amplifier flip-flop (DETSAFF) is for high performance low power design and applications in this paper. In this paper a new dual-edge triggered sense-amplifier flip-flop (NEW DET-SAFF) is proposed for high performance and low power design applications. By setting a dual-edge triggering in the symmetric latch, the NEW DET-SAFF is capable to achieve delay and low power dissipation. The simulations are carried out in tanner tool of 250nm technology. From this it is evident that with the proposed design there is 75.5% in delay and 25.1% reduction in power dissipation. When the switching activity is less, the proposed NEW DET-SAFF shown its superiority in terms of power reduction. During a low switching activity, NEW DET-SAFF can realize up to 85% in power saving.

Keywords: Dual-edge triggering, Clock-gated, high performance, Low- power

INTRODUCTION

In designing high performance semiconducting devices, the parameters like speed, robustness, power consumption, layout area, clock-skew tolerance plays a main role [5]. Flip-flops are important elements for designing these devices; they have a critical influence on these parameters. Flip flops are used as data storing elements. As frequency increases, pulse-based flip-flops are used popularly t as compared with master-slave flip-flops [9]. We have single edge and dual edge triggered flip-flops. In the overall cycle Dual Edge-Triggered Storage Elements (DETSE), capable of capturing signal on both rising and falling edge of the clock [2]. The min idea is to construct the short pulse near the triggering edge. This pulse acts as the clock input for the flip-flop.

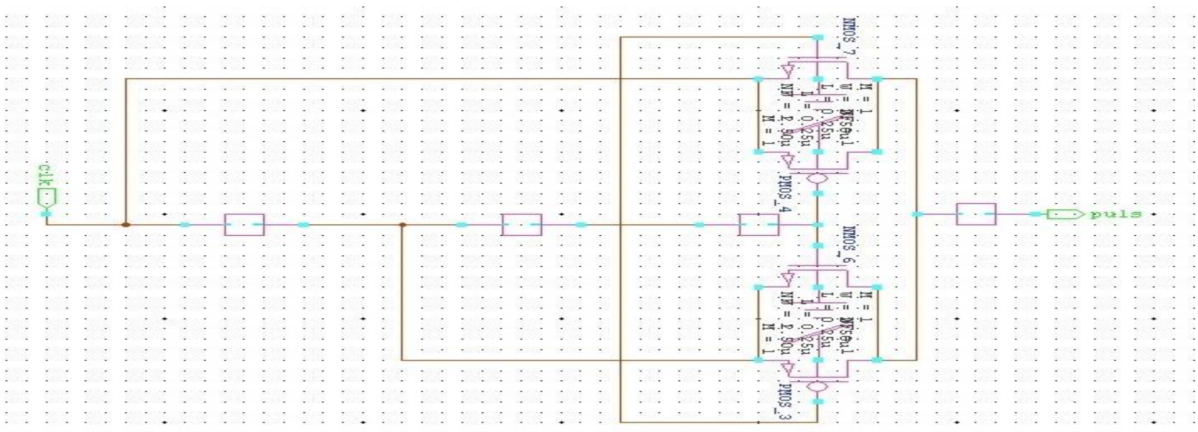
Flip-flops achieve small delay between the latest point of data arrival and output transition so we introduced sense amplifier flip-flop. The sense amplifier based flip-flop is composed of sensing stage and latching stage [3]. The SAFF is characterized by a non-zero setup time, a reduced hold time, a low clock load and true single phase operation.

In this paper, the NEWDETSAFF is capable of achieving low power dissipation and delay. The present operation allows the proposed flip-flop to be faster and more clock-skew tolerant than conventional flip-flops.

REVIEW OF EXISTING DUAL EDGE TRIGGERED FLIP-FLOPS

A. Static output-controlled discharge flip-flop

The schematic of static output controlled discharge flip-flop (SCDFF) [12] is shown in fig.1. In SCDFF we have a static latch and a dual pulse generator. The static latch can capture the pulse signal coming from the pulse generator. The static latch consists of two stages. In the first stage, input D is used to on the pre-charge transistor so that node X follows D during the sampling period. The conditional discharging technique is implemented by inserting a QB controlled by NMOS in the discharge path.



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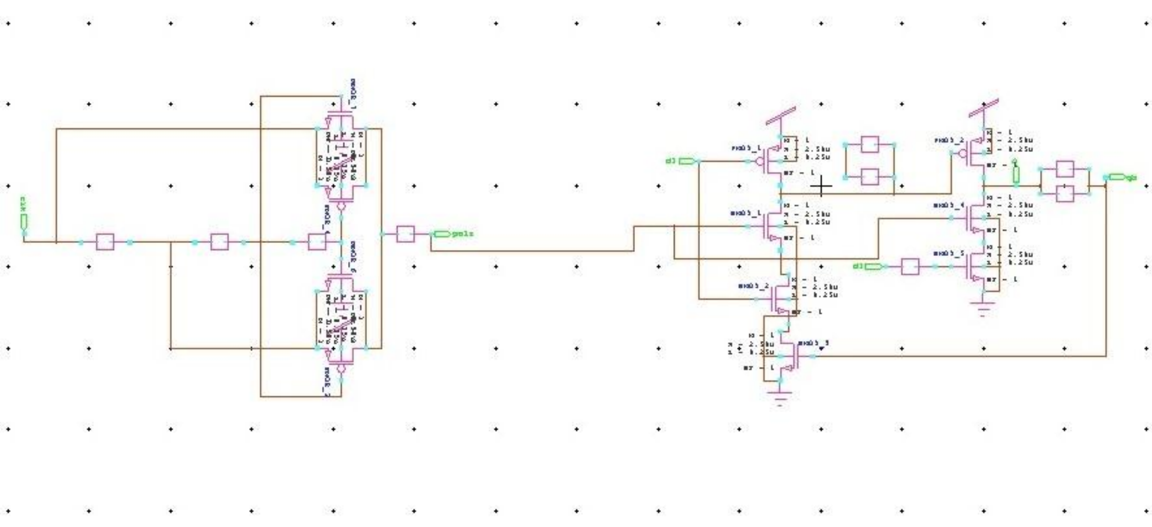

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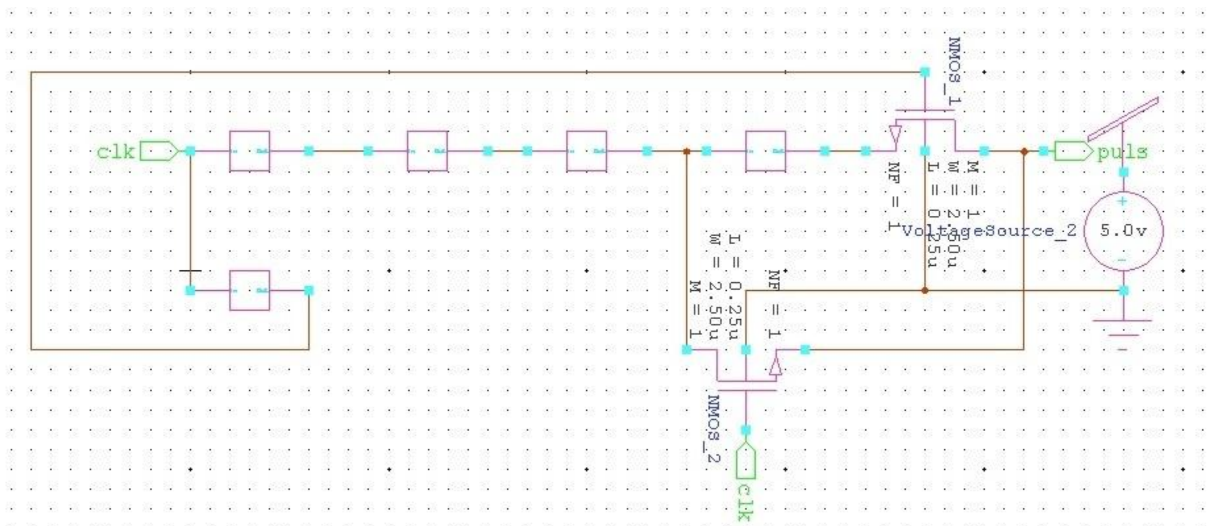
Figure 1: Static output controlled discharge flip-flop (a) dual pulse generator b) static latch

The main advantage of SCDFF is low power consumption and soft edge property. Time delay is the drawback of SCDFF.

B. Dual edge triggered static-pulsed flip-flop

Dual edge triggered static pulsed flip-flop (DSPFF) [10] has dual pulse generator and static latch as shown in fig 2. The pulse generator consists of four inverters which generate delayed and inverted clock signals, CLK2 and CLK3, followed by a pulse signal. In latching stage, once the PULS signal is generated, both pass transistors are turned ON to capture the inputs data so that either SB or RB will be discharged with a small delay since DB and D are fed directly[14]. The PMOS transistors, together with two NMOS transistors, to produce a strong signal avoid a float of nodes SB and RB when the flip-flop is opaque.



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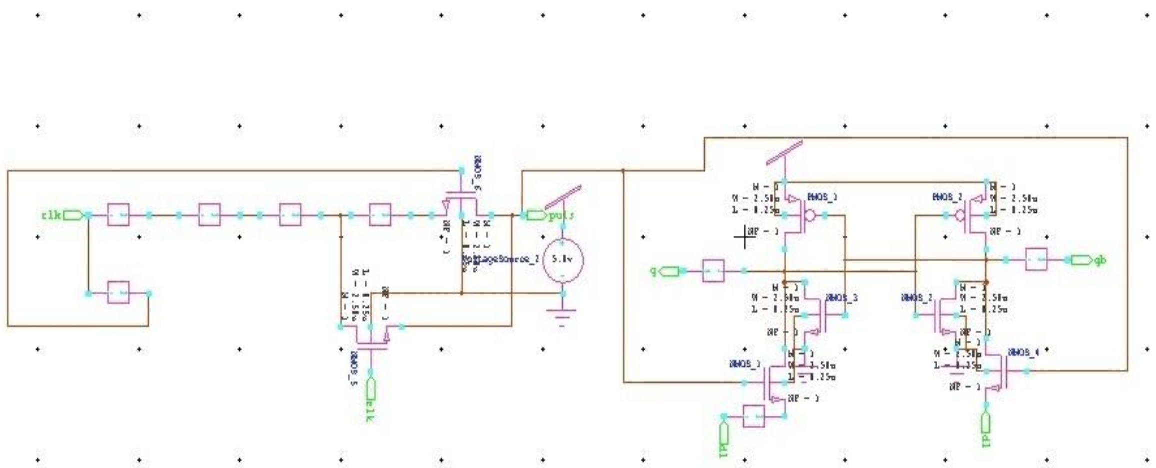

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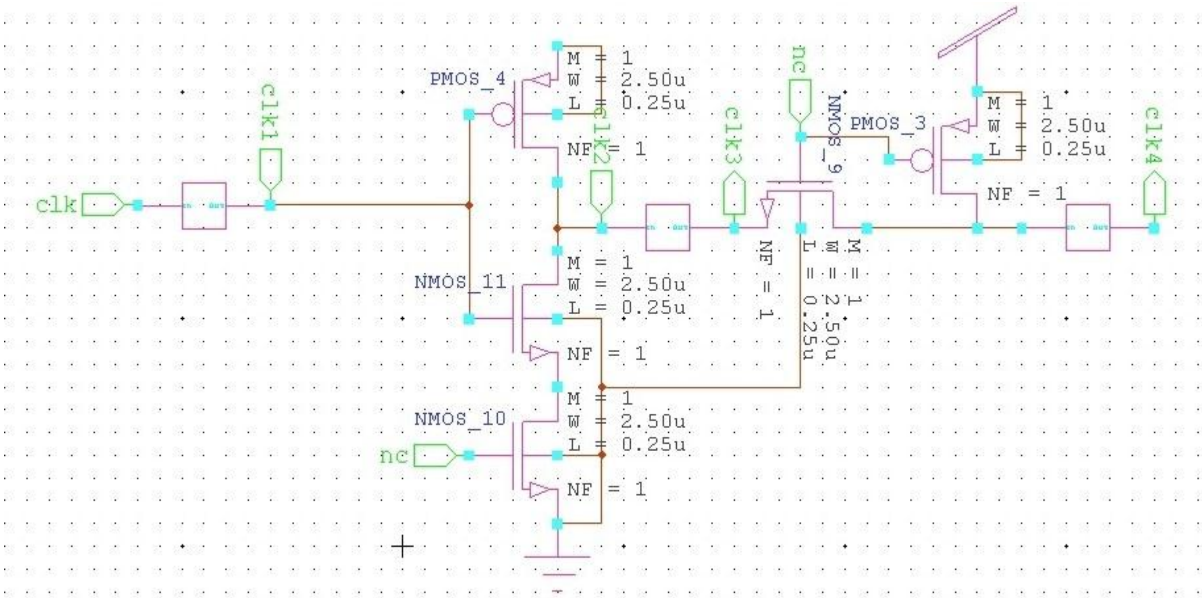
Figure 2: Dual edge triggered static pulsed flip-flop (DSPFF) a) dual pulse generator b) static latch

The advantage of DSPFF is it eliminates unnecessary transitions. It suffers a high leakage current caused by high voltage drop across either the pass transistors when they are in OFF state.

C. Adaptive clocking dual edge triggered sense amplifier flip-flop

ACSAFF[13] consists of three stages: The adaptive clock inverting stage, the front end sensing stage and the Nikolic's latch [11]. Adaptive clock inverter chain is used to disable the internal clocked transistors. In sensing stage, the signal from NC is used to implement the adaptive clock. If input D is different from output Q node then node NC will be pulled up, to on N1 and N2 transistors. The output state in the latching stage will change, when the either of SB or RB will be discharged during this transparent period. CLK3 and CLK4 produces a narrow transparent window is created on the rising and falling edges of the clock. When D is the same as Q node NC is low and the flip-flop is opaque.



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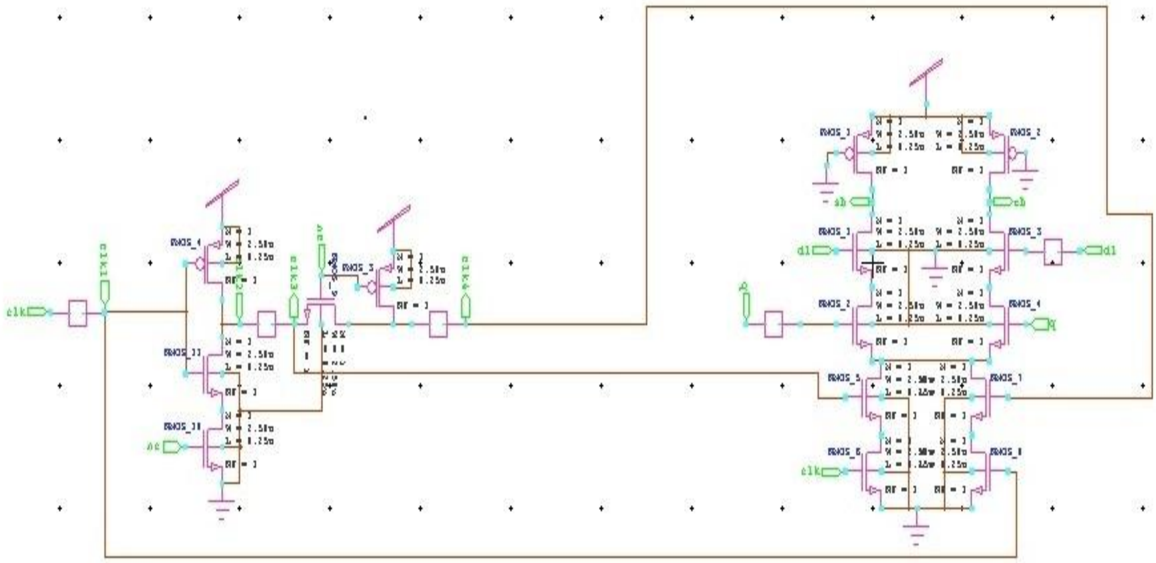

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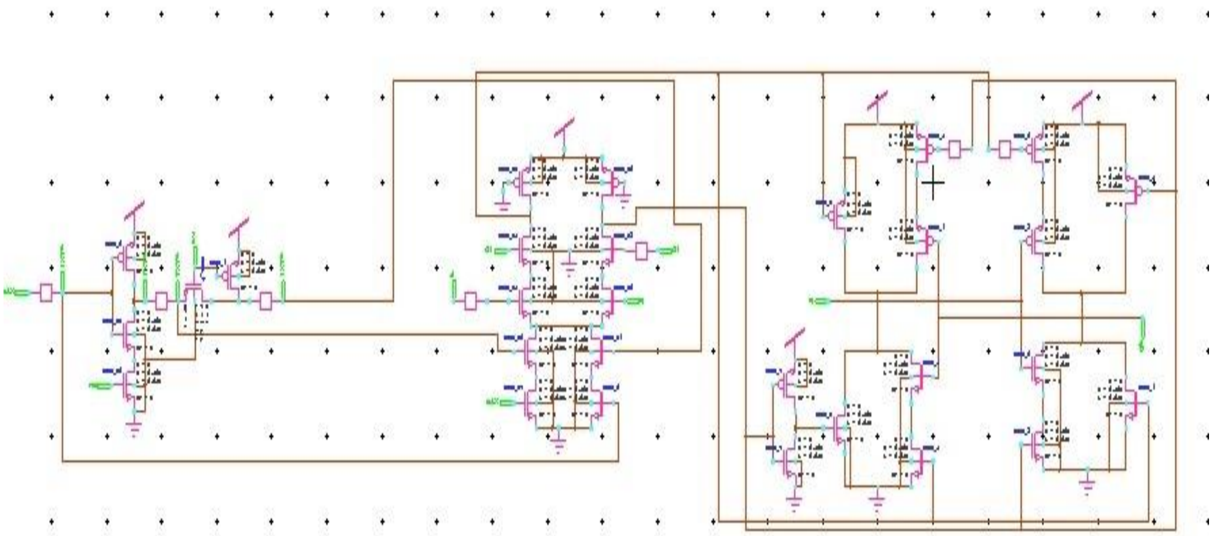

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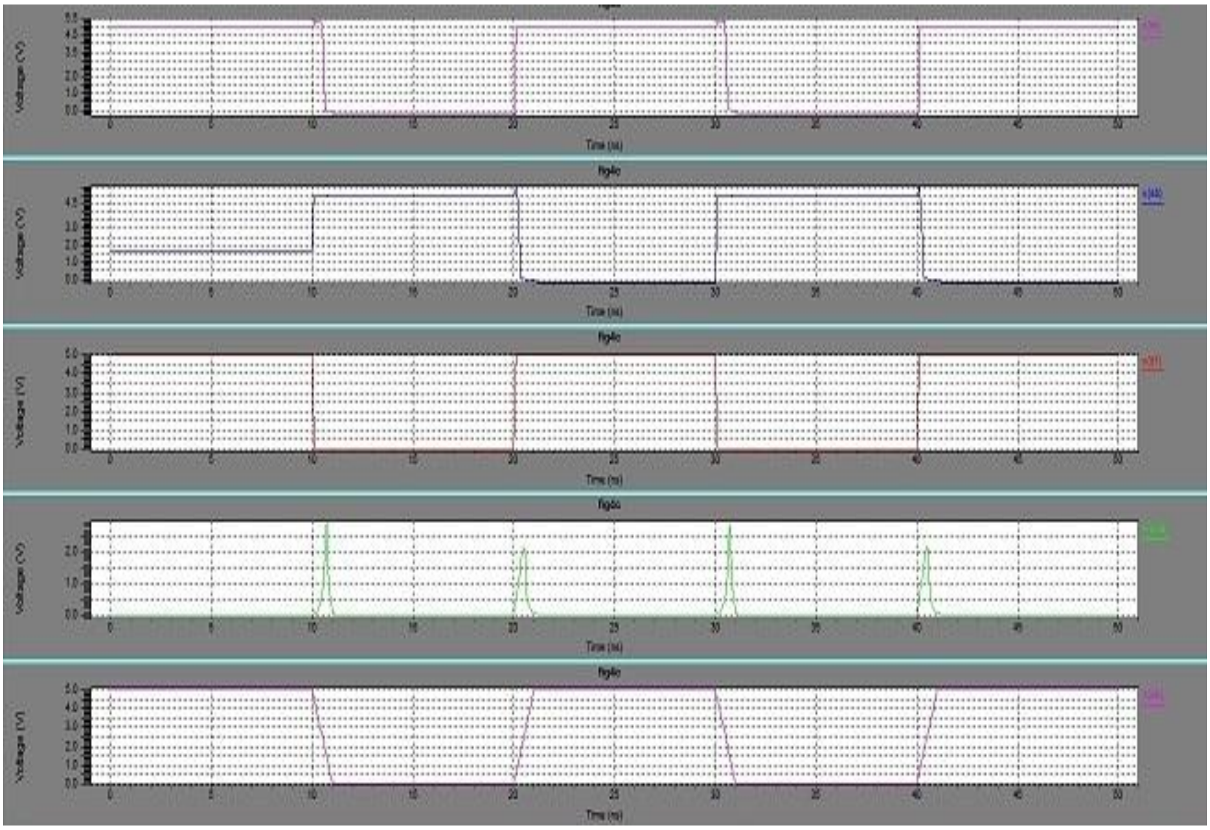
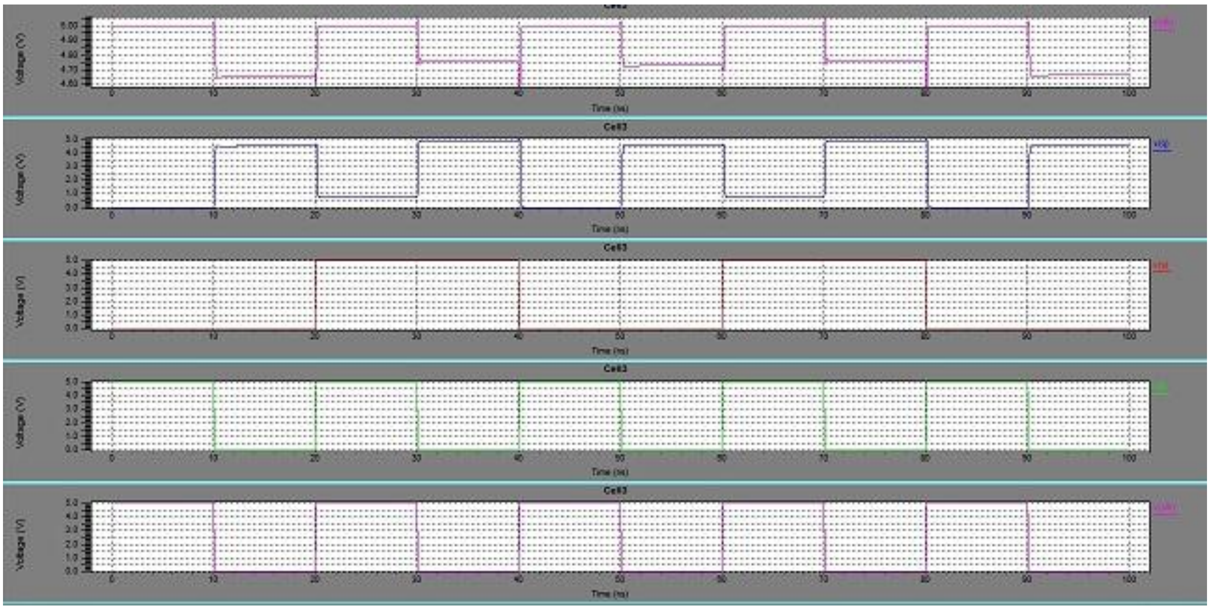
Figure 3: Adaptive clocking dual edge- triggered sense-amplifier flip-flops (ACSAFF) (a) adaptive clocking inverter chain (b) front end sensing stage(c)Nikolic's latch



OUTPUT WAVEFORMS OF ADAPTIVE CLOCKING INVERTER CHAIN

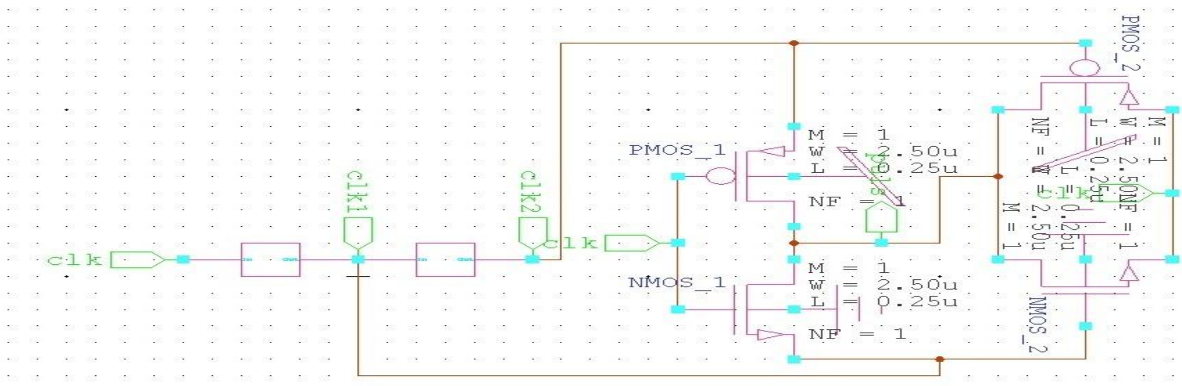


OUTPUT WAVEFORM OF NIKOLIC'S LATCH

The adaptive clocking requires more number of transistors. Once the output is altered with reference to the input then the node NC will be blocked through either of the pull down transistors path. This flip-flop has shown its superiority in terms of power consumption at low switching activity.

D. Modified dual edge triggered sense-amplifier flip-flop

The schematic diagram of the DET-SAFF is shown in Fig.4. The dual edge triggered pulse generator produces a pulse signal which is synchronized at the rising and falling clock edges[13]. For a sense amplifier based flip- flop, in the evaluation phase, when D is low, SB will be set to high, and if D is high, RB will be set to high[14]. In the sensing stage we use conditional pre-charging technique to avoid the number of transitions at internal nodes.



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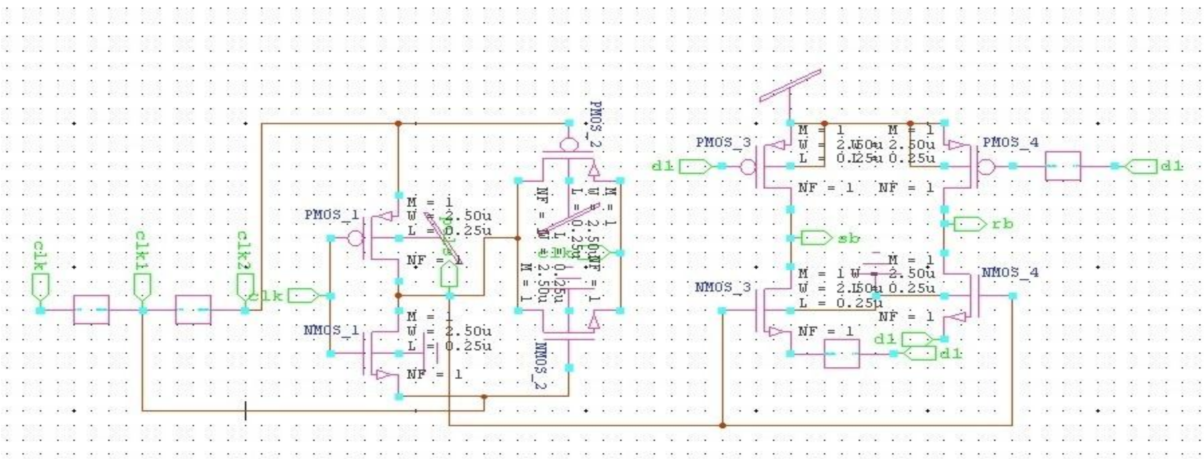

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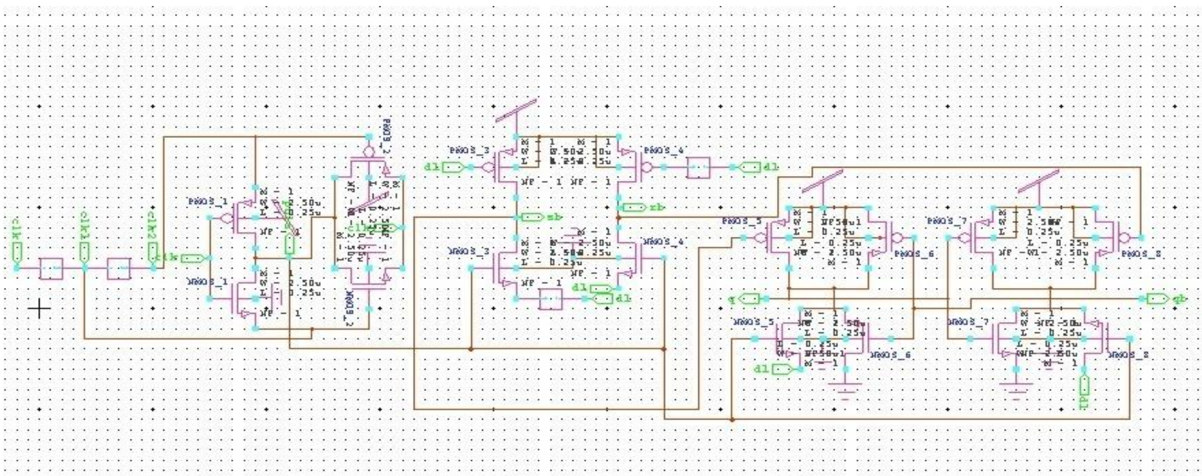

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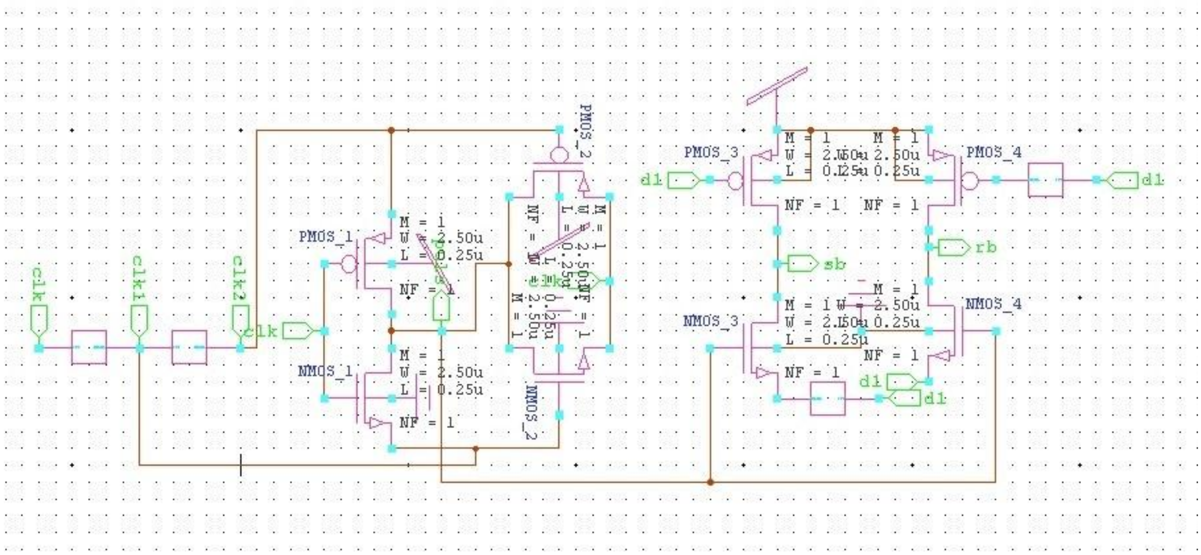
Figure 4. Dual edge-triggered sense-amplifier Flip-Flop (a) Dual pulse generator (b) Sensing and latch stage

The advantage of DET-SAFF is high speed and low power but the unnecessary transitions at low switching activity cause a lot of power to be wasted.

E. Modified clock gated sense-amplifier flip-flop

The schematic diagram of the CGSAFF is shown in Fig.5. It consists of pulse generator and sensing stages of CG-SAFF. The sensing stage is same as the DET-SAFF but the generated pulse will more loaded and nikolic's latch is modified. The inner holding topology is modified to obtain differential outputs, Q1 and QB1, with reduced load capacitances[5]. In the clocking stage, Q1 and QB1 are used to generate X and Y instead of using Q and QB. This helps to improve the performance of CG-SAFF significantly.



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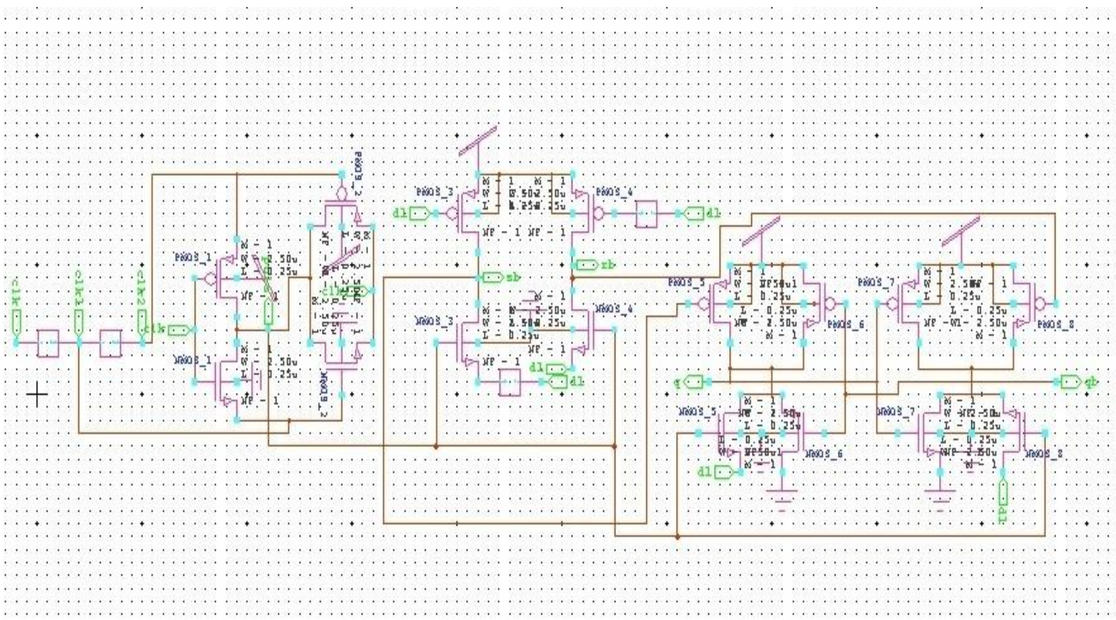

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Figure 5: Modified clock gated sense-amplifier flip-flop: (a) sensing stage, and (b) latching stage.

PROPOSED DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIPFLOP

The schematic diagram of the NEWDETSAFF is shown in Fig.5. It consists of dual pulse generator and sensing stages of DET-SAFF. For achieving low power and high speed, a symmetric latch is developed in latching stage.

Once the PULS is generated from pulse generator then the sensing stage will generate the SB and RB notice transistors Q1 and Q3 resemble the series-connected complementary pair from the inverter circuit. Both are controlled by the same input signal, when the input is "high" the upper transistor will turn OFF and the lower transistor will turn ON, and vice versa. The transistors Q2 and Q4 are controlled by the same input signal (input RB), to the logic levels. The upper transistors of both pairs have their source and drain terminals are connected in parallel, while the lower transistors are connected series.

This arrangement results the output to go "high" or top transistor saturates, and will go "low" only if both lower transistors saturate, the design cross coupling results a latch circuit.

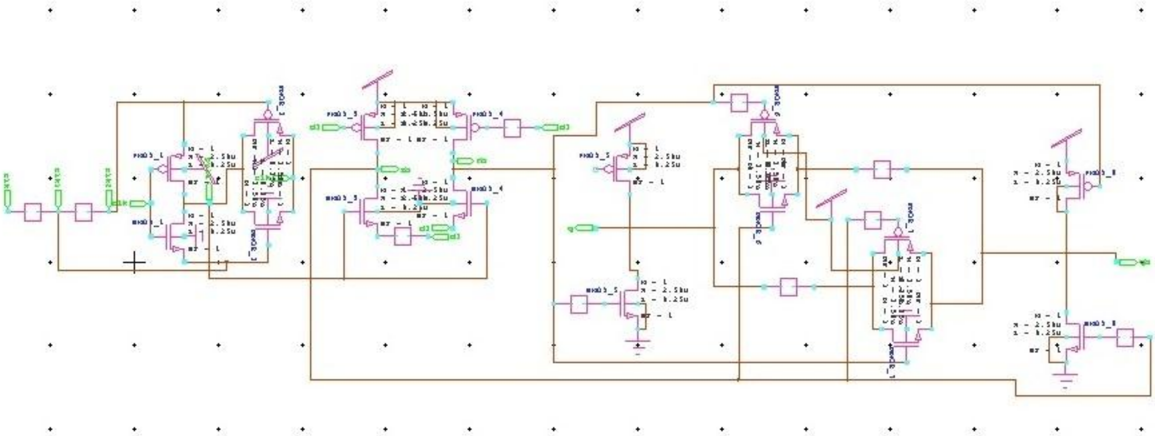

Figure 6: New dual-edge triggered sense-amplifier flip-flop

SIMULATION RESULTS AND PERFORMANCE COMPARISONS

All the flip-flops were designed using Chartered Semiconductor Limited's 0.25µm CMOS process technology, at a supply voltage of 5V, using TANNER TOOLS. The performance of the proposed flip-flop is evaluated and compared with SCDFF, DSPFF, ACSAFF, and DETSAFF. Table I summarize the performance of the reviewed flip-flops and proposed designs, at input switching activity of $\alpha = 1$. The proposed NEWDET-SAFF achieved low CLK-to-Q delay among the flip-flops.

Designs	SCDFF	DSPFF	ACSAFF	DETSAFF	MDETSAFF	NEW DET-SAFF
Clk to Q delay(ps)	619.80	886.7	598.5	192.36	137.877	37.877
Min D to Q delay (ps)	620.40	572.9	803.1	197.36	1938.19	178.19
Rise time(ps)	103.33	146.7	218.89	111.02	92.02	32.02
Fall time(ps)	97.981	800.0	111.02	50.452	88.751	49.751
Total Power dissipation(nw) at 25% switching activity	39.5652	36.2655	33.0154	31.5423	27.6426	25.8345
# of transistors	29	24	39	22	23	22

APPLICATION

The application of this new dual edge triggered flip-flop is counters and shift registers.

A shift register is digital data storage. As applied to digital circuits, a shift register is a series of flip-flops based on sequential clock timing. Shift registers are high-speed circuits.

Primarily, a shift register moves bits of data either left or right along a circuit, depending on structure and design of the circuit.

Now we are discussing about shift register below, the schematic diagram of serial in parallel out shift register is shown in fig 7. We are using four D FLIP-FLOPS in this design. The output waveforms of the SIPO shift register is shown in fig 8.

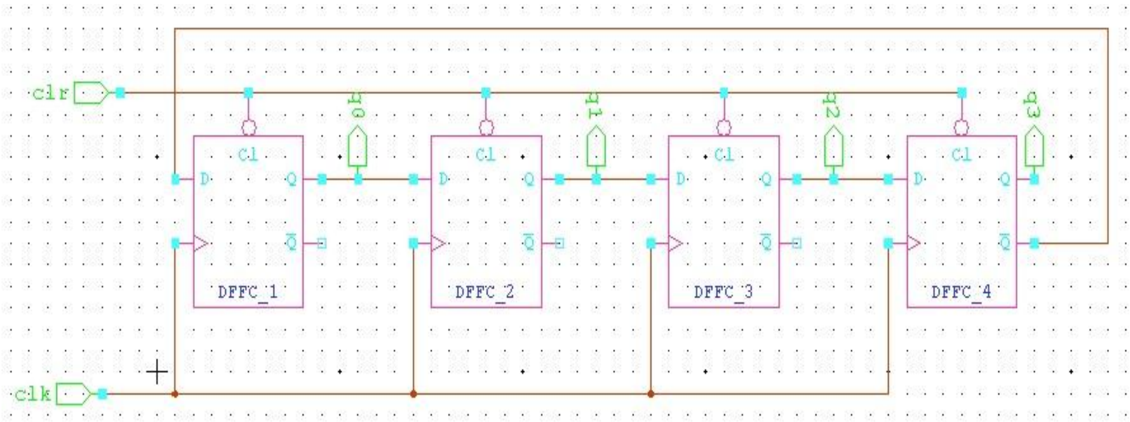

Figure 7: Serial in parallel out shift register

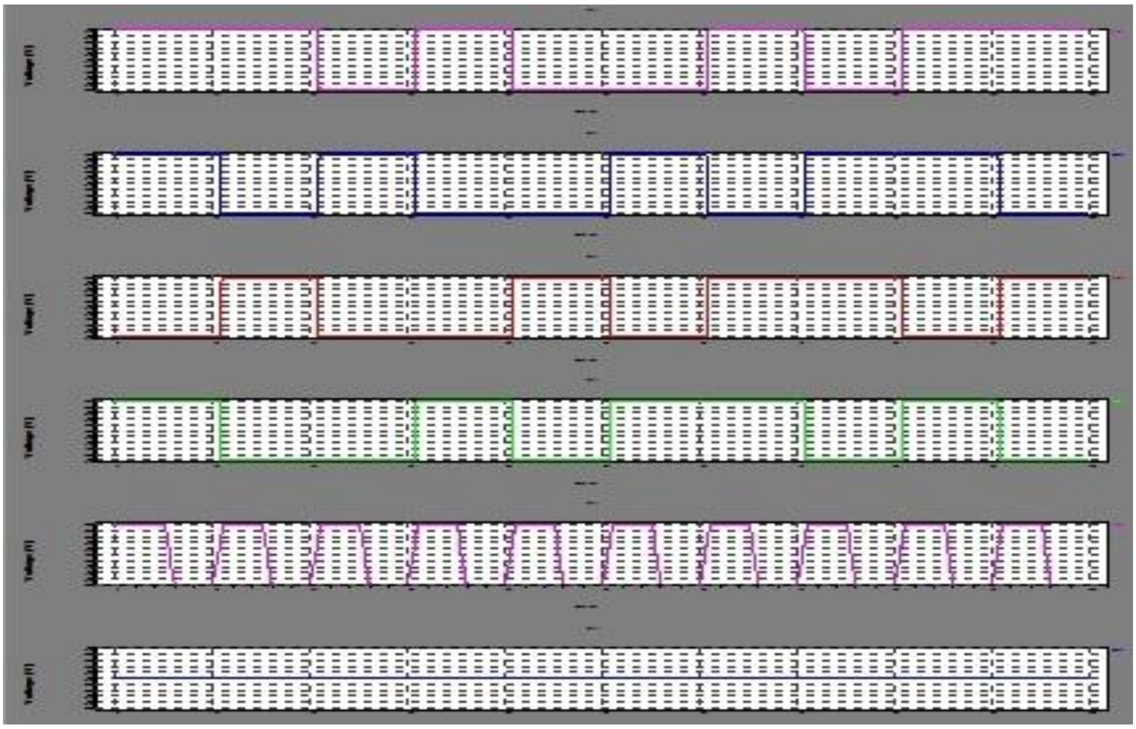

Figure 8. Output waveform of SIPO Shift registers

CONCLUSION

In this paper a new technique, conditional precharge, is proposed. This technique is incorporated in the dual edge triggered sense amplifier flip-flop and a new flip flop named NEW DET-SAFF is proposed to reduce the delay and power dissipation in flip-flops. With a data switching activity of 50%, the new flip-flop can save up to 36% of the energy with the same speed as that for the fastest pulsed flip-flops. NEWDET-SAFF is suitable for both speed critical paths and speed-insensitive paths for energy-efficiency. This new design is developed to reduce the power dissipation and delay when compared to the clock gated sense-amplifier flip-flop up to 22.1% and 76.5% respectively.

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