Design of a New Dual Dynamic Flip-flop with Low Power and Low Area

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Abstract – The fast growth of the power density in integrated circuits has made area and power dissipation as the vital design measures. To store data latches and flip-flops are the basic elements. Less power will be dissipated for a classic structured Dual Dynamic Flip-Flop (DDFF), as mentioned in an open literature. In this paper DDFF is designed which dissipates less power due to large pre-charge node capacitance. In this number of transistors required to design are reduced. From the results by comparing power analysis and performance, the proposed design is suitable for high performance digital designs where area and power dissipation are mainly considered. The proposed flip-flop reduces power dissipation up to 60-70% and area up to 40% compared to conventional flip-flops. By using proposed flip-flop, a Serial in serial out (SISO) Shift register is designed using TANNER Simulation Tool, with Schematic editor 250nm technology.

Index Terms – DDFF, high speed, low power, small area, power dissipation, high-performance, dynamic logic.

1. INTRODUCTION

Over the past decade, in VLSI chips power consumption has been increasing constantly. Advances in the VLSI technology shows that on chip transistors are increased about 40% and the clock frequency increased about 30% every year. On the other hand the reason for power consumption is lack of advancements in the cooling systems. A digital logic circuit is called as sequential circuit if its supports memory (Flip flop). Most of the portable devices consist of one or more sequential circuits. Thus a low power dissipating and area efficient VLSI systems can be designed.

Basic building block of many electronic circuits is a Flip flop which stores a logical state of one data in response to a clock pulse. A Flip flop can be made to trigger either at positive/Negative level or raising/ falling edge triggering. These flip flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period. The data in the flip flop is available to other combinational or sequential circuit only upon the rising or falling edge of a clock signal. In this paper three new D flip flops architectures are proposed to achieve low power consumption and efficient area and the results are compared with the conventional flip-flops.

A) Static Power Dissipation:

The static power components play a vital role when the circuits are at rest, i.e. when there is no activity in the circuits and they are all biased to a specific state. It includes sub threshold and reversed biased diode leakage currents. Due to the necessary but harmful (in a leakage power sense) down-scaling of threshold voltages, the sub threshold leakage is becoming more and more pronounced. Below the threshold voltage, in weak inversion, the transistors are not completely off. The sub threshold current has a strong dependence on the threshold voltage.

b) Dynamic Power dissipation:

The dynamic power dissipation, $P_{dynamic}$, is due to capacitor charging and discharging in the circuit. The output capacitor C_L represents the cumulative effect due to parasitic capacitances of the NMOS and PMOS transistors (source- and drain-diffusion to bulk), the capacitance associated with internal and external wires of the inverter cell, and the input capacitance (gate to bulk) of the circuits driven by the inverter. Therefore, the dynamic power dissipated by a CMOS inverter over a time interval can be computed by:

The total power dissipated in generic digital CMOS gate is calculated by using equations (1 - 4)

$$P_{total} = P_{dynamic} + P_{shortcircuit} + P_{static} \quad (1)$$

$$P_{dynamic} = P.C_L.f.V_{DD}^2 \quad (2)$$

$$P_{shortcircuit} = I_{peak}.t_{SC}.V_{DD}.f \quad (3)$$

$$P_{static} = I_{static}.V_{DD} \quad (4)$$

Where p = Change state probability of gate.

f = frequency

C_L = Load Capacitance

V_{DD} = Supply Voltage

I_{peak} = Maximum current during the status of gate

t_{SC} = sort circuit time & I_{static} = static current

The three major components of power dissipation in complementary metal–oxide–semiconductor (CMOS) circuits are Switching Power, Short Circuit Power and Static Power. Dynamic power creates the majority of the power dissipated in the CMOS VLSI circuits. It is due to charging or discharging of load capacitances in a given circuit. Power consumption of the circuit can be reduced by reducing any of the component parameters.

2. EXISTING WORK

A. POWER PC 603 FLIP-FLOP:

Flip flops can be grouped into static and dynamic design styles which includes the master- slave designs, such as the transmission gate based master-slave flip-flop and the PowerPC 603 master-slave latch. Power PC stands for Performance Optimization with Enhanced RISC Performance Computing. It dissipates comparatively lower power and also having a low clock-to-output (CLK-Q) delay. In synchronous systems, the latching elements have the delay overhead which is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here, D-Q delay is the combination of CLK-Q delay and the setup-time of the Flip-Flop.

The PowerPC 603 master-slave latch [1] is shown in Fig 1. It has the advantages of having a low-power keeper structure and also a low latency direct path. It is one of the fastest classical structures and its main advantage is the short direct path and low power feedback structure. The large load on the clock will greatly affect the total power dissipation of the flip-flop. The PowerPC 603 flip-flop is the transmission gate flip-flop, it has a fully static master–slave structure, which is designed by cascading two identical pass gate latches and provides a short clock to output latency. It does have a worse data-to-output latency because of the positive setup time and its sensitivity to clock signal slopes and data feed through is another major concern when using it. The large D-Q delay resulting from the positive setup time is one of the disadvantages of this design. Also, the large data and CLK node capacitances make the flip flop design inferior in performance. Despite all these shortcomings, static designs still remain as the low power solution when the speed is not a primary concern.

The second category of the flip-flop design are the dynamic flip-flops which includes the modern high performance flip-flops. These are purely dynamic designs as well as pseudo-dynamic structures. The latter, these designs has an internal precharge structure and a static output, deserves special attention because of their distinctive performance improvements. They are called the semi-dynamic or hybrid structures, because they consist of a dynamic frontend and a static output.

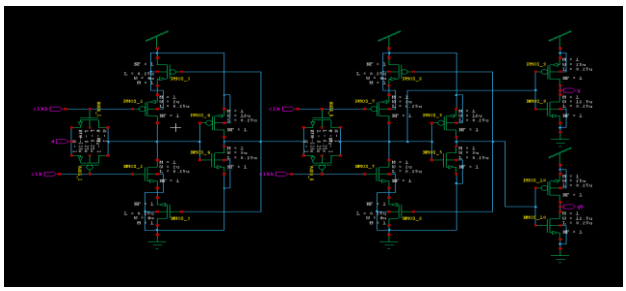

Fig 1: PowerPC 603 flip-flop.

B.HYBRID LATCH FLIP-FLOP (HLFF):

The hybrid latch flip-flop (HLFF) is one of the fastest dynamic flip-flop structure, which dissipates less power. It is robust to clock signal slopes, but it does have a positive hold time. HLFF is very suitable for high performance system as shown in fig 2.

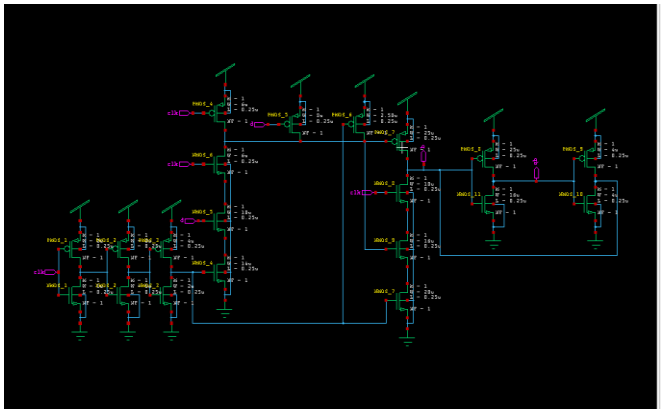

Fig 2: Hybrid Latch Flip Flop (HLFF).

This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This sharp pulse is generated at the positive rising edge of the clock and delayed version of the clock [2]. Due to this large hold time requirement incorporating complex designs in HLFF is a difficult process.

C. SEMI DYNAMIC FLIP-FLOP (SDFF):

SDFF is the fastest classic hybrid structure, but it consumes more power as compared to HLFF, because of the large CLK load as well as the large precharge capacitance. HLFF is not the fastest but has a lower power consumption compared to the SDFF due to the longer stack of nMOS transistors present at the output node (Fig. 3) makes the operation slower than SDFF and causes large hold-time requirement. The SDFF design consumes more power it is efficient for

incorporating complex logic functions such as AND, OR and MUX logics.

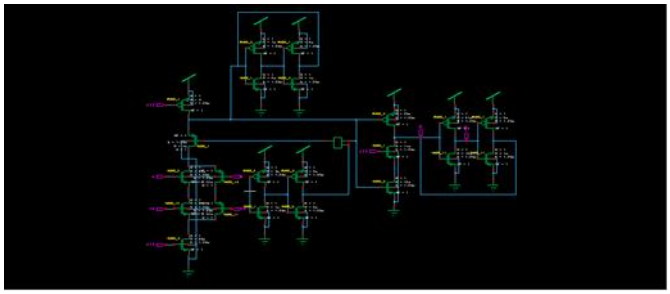

Fig 3: Semi Dynamic Flip-Flop (SDFF)

D.CONDITIONAL DATA MAPPING FLIP-FLOP:

Fig 4 is Conditional Data Mapping Flip-Flop (CDMFF), it is the most efficient design to reduce the redundant data transitions in the flip-flop. CDMFF uses an output feedback structure to conditionally feed the data to the flip-flop which reduces the overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Since there are no added transistors in the pull down NMOS stack, the speed of the performance is not greatly affected. But due to the presence of three stacked NMOS transistors at the output node, similar to HLFF design, and the presence of conditional structures in critical path increase the hold time requirement and D-Q delay of the flip-flop [3]. Also, the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation at higher data activities.

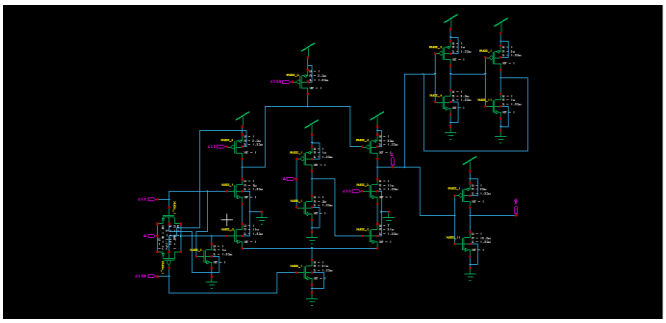

Fig 4: Conditional Data Mapping Flip-Flop (CDMFF).

E.CROSS CHARGE CONTROL FLIP-FLOP (XCFF)

The cross charge control flip-flop (XCFF) reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors as shown in fig 5. The total power consumption is greatly reduced without any degradation in speed because; only one of the two dynamic nodes is switched during one clock cycle [4]. XCFF has a comparatively lower CLK driving load.

The disadvantage of this design is that, the redundant precharge at node X2 and X1 for data patterns containing more 0s and 1s respectively. Due to the conditional shutoff mechanism, the large hold time requirement appears at the output, and a low to high transition in the CLK when the data is low, causes charge sharing at node X1. The problem of charge sharing becomes very high when complex functions are incorporated into the design [5].

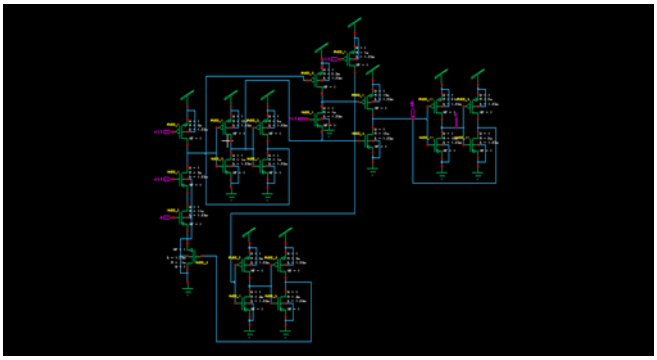

Fig 5: Cross Charge Control Flip Flop (XCFF).

F. DUAL DYNAMIC FLIP-FLOP (DDFF):

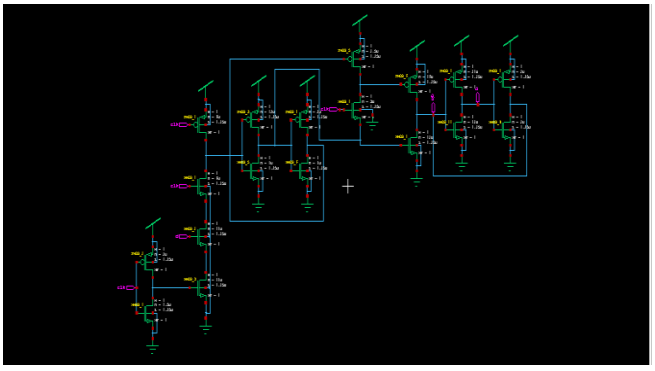

Fig 6: Dual Dynamic Flip-Flop (DDFF)

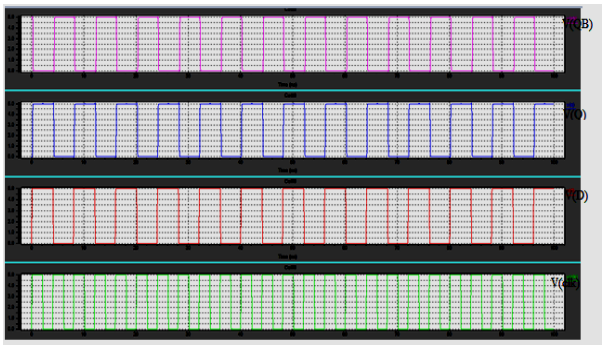

Fig 7: Waveform of DDFF

The dual dynamic flip-flop (DDFF) acts like static and dynamic circuit and the schematic is shown in below fig 6. The operation of DDFF is based on the dynamic logic

principles. The working of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when CLK is low. This design consumes less power as compared to existing static and dynamic flip flops. In DDFF, due to the feedback structure at the output node, the switching for more data patterns is inefficient [7, 8]. It is efficient for incorporating complex logic functions such as AND, OR and MUX logics

3. PROPOSED MODELLING

The proposed Flip Flop consists of less number of transistors and consumes very less power as compared to DDFF design as shown in fig 8. This structure is efficient for incorporating complex logic functions such as AND, OR and MUX logics.

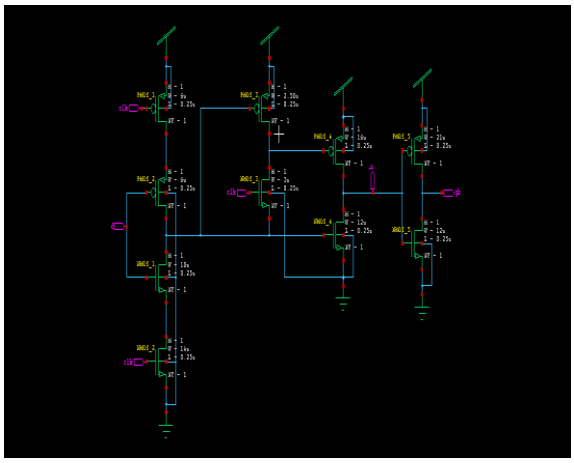

Fig 8: Proposed Flip-Flop

4. APPLICATIONS

SHIFT REGISTERS

A shift register is digital data storage. The data can be the letters to be displayed on a TV screen, numbers in a computer or calculator, intermediate values in a digital filter or part of an elaborate code or sequence. Shift registers are made up of individual stages. Each stage can store one bit of information, called a binary 1 or a 0, and usually corresponding to a "yes" or "no" or else perhaps a "present" or "absent" command. Four bits together can represent a decimal number, while six bits together can handle one ASCII character, and so on. In a shift register, the contents can be moved or shifted so that the contained information is marched one and only one stage at a time through the device. The shifting process is called clocking and one or more clocks can be involved in completing the shifting operation.

Serial-In Parallel-Out (SIPO) Shift Register:

In Serial-in Parallel-out (SIPO) shift register. The four data bits will be shifted in from “data in” by four clock pulses and is available at QA through QD.

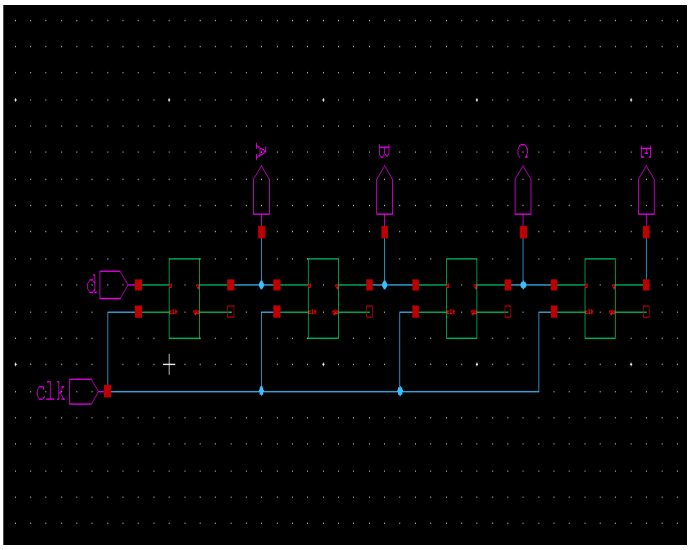

Fig 9: Serial-In Parallel-Out (SIPO) shift register using DDFF.

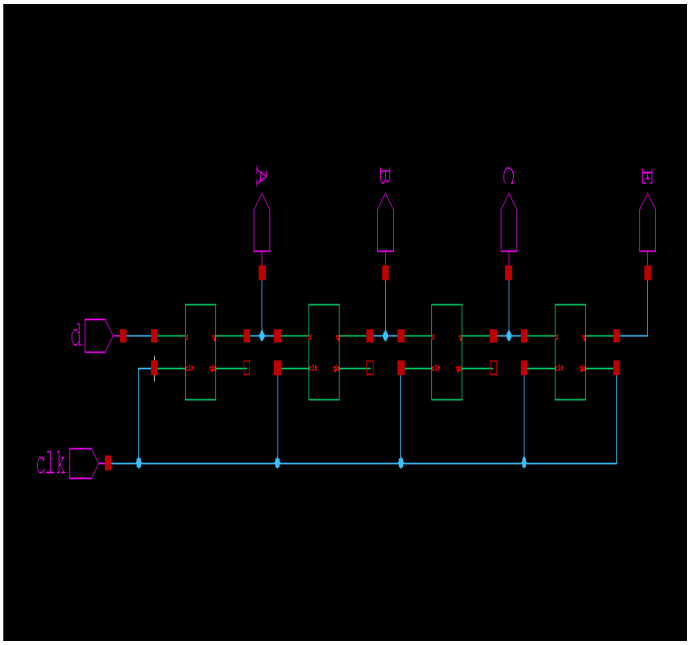

Fig 10: Serial-In Parallel-Out (SIPO) shift register using Proposed Flip Flop.

5. SIMULATION RESULTS

In order to compare the performance of proposed flip-flop with existing flip-flop designs, all the circuits are simulated in 250nm CMOS technology of mentor graphics tools with a supply voltage of 1.2V. Table I illustrates the performance comparison of existing and proposed flip-flops and table II summarizes comparisons of SIPO shift registers.

TABLE 1: PERFORMANCE COMPARISON OF VARIOUS FLIP-FLOPS

Flip-Flop	Number of transistors	D-Q DELAY	CLK-Q DELAY	RISETIME	FALLTIME	POWER DISSIPATION
POWERPC 603	22	60.392ns	55.672ps	82.675ps.	150.56ps	24.561NW
HLFF	20	58.670ns	875.63ps	172.627ps	70.008ps	17.153NW
CDMFF	22	165.50ps	835.50ps	191.63ps	351.22ps	15.631NW
XCFF	21	80.918ps	58.375ps	54.954ps	35.70ps	18.4337NW
DDFF	18	362.67ps	852.22ps	202.70ps	356.28ps	17.77NW
Proposed Flip-Flop	10	255.13ps	343.21ps	123.46ps	134.46ps	5.689NW

TABLE II: COMPARISION RESULTS OF SIPO SHIFT REGISTERS

	CLK-Q DELAY	RISETIME	FALLTIME	POWER DISSIPATION
SIPO(XCFF)	546.352ns	52.567ps	45.728ps.	68.218NW
SIPO(DDFF)	443.69ps	63.322ps	70.212ps	53.756NW
SIPO(proposed flip-flop)	635.53ps	125.23ps	52.63ps	32.187NW

6. CONCLUSION

In this paper flip-flop is proposed based on DDFF design. The proposed flip-flop architecture exhibits reduction in the power dissipation up to 50-60% and delay up to 86% than the conventional flip-flops. A SIPO shift register is designed using conventional and proposed flip-flop. The SIPO shift register designed with proposed flip-flop exhibits 83% of reduction in the power dissipation.

As a future work, complex logic functions can be incorporated into the proposed flip-flop.

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