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An Efficient VLSI Implementation of High Speed 1024 AES Using Cryptography

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Abstract
Cryptography is the technique to improve the signal security Cryptography is the technique of data to reduce the hacking effects. The for the transmission of data to reduce the hacking effects. The for the transmission of data the two stages they are symmetric cryptography is mainly done in two stages they are symmetric cryptography. The plain cryptography is mainly dollar cryptography. The plain text is cryptography and asymmetric cryptography side some text is cryptography and asymmetric and at the decryption side same key is encrypted with the key and at the decryption. The encryption encrypted with the displacement on the encryption is done used to extract the original information. The encryption is done in the different symmetric key algorithms like DES, RC2, RC4, AES etc. are improved to secure the information. In this paper a new algorithm is used to improve the signal security to avoid the hacking effects. The proposed technique is implemented in the 1024 bits along with the 1024 key and the decryption is also done with the same key to obtain the plain text. In the proposed method the signal security is improved while varying the different key lengths, due to this hacking is not possible. The proposed technique achieves high speed and signal security compared with previous AES algorithms.

Key words: Advanced Encryption Standard, RC4, Plain text, Cryptography.

Introduction

Cryptography is used to encode the information in a very high secure manner and when the data is highly confidential key is wave either by the data. Using the key is also done in two ways either by using the public key or the private key. The public key is used for the known purpose and for the transmission of any law is transmission of open secured information. The private key is used for the transmission of open secured information. used for the transmission of very confidential data and these public keys are only because the Here public keys are only known by the sender and receiver. Here the information is called a by the sender and receiver. the information is called as the plain text and the plain text is encrypted with the ker and the plain text and the plain text and the plain text is encrypted with the key to obtain the encrypted data. The encrypted that is transmitted the encrypted data. encrypted that is transmitting is unable to read and the in unable to read and the in unable to read and the in unreadable format and not understandable format. At the encrypted message contains only different symbols which the

receiver side the encrypted messaged is decrypted with the Responsibility of contents of this paper rests upon the authors and not upon the Editor & Publical and not upon the Editor & Publisher.

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same key to extract the original information called as plain

Previously Blowfish algorithm is used to encrypt the data but using these techniques two different keys are used in the encryption process. Due to the use of asymmetric use of keys the speed of the encryption is getting reduced and the signal is also easy to hack. Hence the encryption of 128 bit plain text along with the key is unsatisfactory and to overcome this new 1024 AES algorithm is implemented to improve the signal security along with the speed. Hence the results show that the proposed architecture is going through odd and even substitutions only. The complete data is splatted into two parts and the first half will perform the left shift operations and the second half will do the right shift operations. The key is also used here to reduce the rounds hence instead of sixteen rounds in this architecture there are only eight rounds are using to obtain the encrypted data. The proposed design consists of AES algorithm with a little reduction of the plain text and the key size. Hence for the 1024 AES used 512 bits to implement the encryption process.

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To understand the AES in an easier manner different AES architectures are studied in the literature. Here, the AES architectures are implemented which not more than 128 bit such as the work is presented in [8] [9] [10]. Previously different encryption algorithms are implemented to improve the signal security. The main purpose of designing the AES is to avoid the data hacking and information leakage. Different encryption algorithms are implemented and studied for the better understanding of the AES hardware implementation in [3] [7] [18] [19] [20]. In these papers different AES architectures are implemented, analyzed and shows the improvement in terms of area consumption, delay and power consumption along with the signal security. Theauthors in [7] and [8] have given a brief comparison of the FPGA hardware performance of the AES candidates.

At present, AES shows the better signal security compared to all the previous encryption algorithms. When there is a transmission of transmission of confidential and high priority data to the

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