ISBN: 978-93-5780-385-4

Low Power and Area Efficient Flip Flop With Embedded Logic Module

Ms. Sheik Shabeena [1] Mr. R. Suneel Kumar[2]
[1,2]Assistant Professor, Dadi Institute of Engineering and Technology, JNTUK

Abstract: As number of modules per chip is increasing, number of transistors in a chip increases resulting in increase in area and power dissipation. Area and power dissipation problems can be most effectively addressed if the basic building blocks of the circuit are designed for lower power dissipation and occupy less space. Flip- Flop, which is basic building block, plays a major role in design of complex systems. From the open literature, Semi Dynamic Flip-Flop (SDFF) and Dual Dynamic Flip-Flops (DDFF) are classic structures which are efficient for incorporating complex logic functions. In this paper, a new low power and area efficient flip-flop with Embedded Logic Module (ELM) is proposed. The proposed Flip-Flop reduces 50% to 60% of power dissipation as compared to conventional flip-flops and delay up to 86% is also reduced. Serial in Parallel out (SIPO) shift register is designed with the proposed flip-flop which exhibit low power dissipation. The simulations are done in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology.

Index terms: SDFF, DDFF, high speed, low power, embedded logic.

Introduction

Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of VLSI circuits. As VLSI circuits continue to evolve and technologies progresses, the level of integration is increased and higher clock speed is achieved. Higher clock speeds, increased levels of integration and technology scaling are causing unabated increases in power consumption. As a result, low power consumption is becoming a critical issue for modern VLSI circuits. Furthermore, power dissipation, dynamic and static, has become a limiting factor for transistor performance, long term device reliability, and increasing integration.

978-93-5780-385-4

-flop is a data storage element. The operation of the flip- is done by its clock frequency. When multistage flip- is operated with respect to clock frequency, it processes high clock switching activity and then increases time ncy. Therefore it affects the speed and energy ormance of the circuit. Various classes of flip-flops have proposed to achieve high-speed and low-energy ation. From the open literature, Semi Dynamic Flip-Flop FF) and Dual Dynamic Flip-Flops (DDFF) are classic ctures which are efficient for incorporating complex logic tions [1].To achieve low power dissipation along with efficiency, a new low power and low area Flip-Flop with edded Logic Module (ELM) is proposed and is compared the conventional Flip-Flops.

Dissipation

dissipation is recognized as a critical parameter in n VLSI design field. The design of portable devices es consideration for peak power consumption to ensure lity and proper operation. However, the time averaged is often more critical as it is linearly related to the life. There are four sources of power dissipation in CMOS circuits: switching power, short-circuit power, power and static power. The following equation es these four components of power:

ddVsfck+Isc

geVdd+
Vdd(1)
tatic=
dVsfck ,
mic= IscVdd ,
ge= IscVdd
ort-circuit = IstaticVdd

ional Flip-Flop
tures
Dynamicflip-Flop (Sdff)

mic flip-flops include the modern high performance . They are divided into purely dynamic designs and