DADI INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by A.I.C.T.E., New Delhi & Affiliated to JNTUK, Kakinada)

NAAC Accredited Institute

An ISO 9001:2008, ISO 14001:2004 & OHSAS 18001:2007 Certified Institute.

NH-5, Anakapalle – 531002, Visakhapatnam, A.P.

Phone: 08924-221111 / 221122/9963981111, www.diet.edu.in, E-mail: info@diet.edu.in

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Question Bank

Name of the Faculty: D.RAVI NAYAK

Subject: Digital Communications

Regulation: R16

III Year – I SEMESTER

UNIT I: PULSE DIGITAL MODULATION

1 a) Explain delta modulation in detail with suitable diagram. [10M]

b) Given a sine wave of frequency fm and amplitude Am applied to a delta modulator having step size _. Find the condition on Am for which slope overload distortion will occur

2 a) Draw the block diagram of ADM system? Explain each block.

b) What are the noises in PCM? Derive an expression for quantization in noise in PCM.

3 a) Explain quantization error and derive an expression for maximum SNR in PCM system that uses Linear quantization.

b) In a binary PCM system, the output signal to quantizing noise ratio is to be held to a minimum value of 40dB. Determine the number of levels and find the corresponding signal to quantizing noise ratio.

4 a) A Television signal having a bandwidth of 10.2 MHz is transmitted using binary PCM system. Given that number of quantization levels is 512.Determine:

(i)Code Word length (ii) Transmission Bandwidth (iii) Final bit rate (iv) Output signal to quantization noise ratio

b) What is slope overload and granular noise distortions are removed in ADM? Explain

5 a) What is the necessity of non-uniform quantization and explain companding. [10M]

b) If mp = 20V and 256 quantizing levels are employed, what is the voltage between levels when there is no compression? For μ = 255, what is the smallest and what is the largest effective separation between levels?

6 a) Discuss in detail the noise effects in delta modulation

b) Briefly list out the differences between PCM and DM.

UNIT II: DIGITAL MODULATION TECHNIQUES

1 (a) Draw the block diagram of DPSK modulator and explain how synchronization problem is avoided for its detection.

b) Write the power spectral density of BPSK and QPSK signals and draw the power spectrum of each.

2. (a)Explain the generation of M-ary ASK with a neat block
b) Explain the principle of QPSK system. Compare binary PSK and QPSK schemes.

3 (a) Explain with neat block diagram the generation and recovery of BPSK
b) What are power spectra? Explain power spectra of BPSK and BFSK signals along with graphs.

4. Determine the bandwidth required for M-ary FSK system. Draw the geometrical representation of M-ary FSK signals and find out the distance between the sign
b) Sketch the QPSK waveform for the sequence 1101010010, assuming the carrier frequency equal to bit rate.

5. (a)Discuss the ASK system in detail

b) Draw the block diagram of the DPSK modulator. Explain how the synchronization problem is avoided in this.

UNIT III: DATA TRANSMISSION

1.a) Explain about ASK system and derive the relation for error probability of binary ASK.

b) A binary receiver system receives a bit rate of 1Mbps. The waveform amplitude is 5mV and the noise power spectral density is 0.5x10-11 W/Hz.
Calculate the average bit error probability if the modulation schemes are ASK, FSK and PSK.

2. a) Draw and explain the coherent system of signal reception. [10M]
b) Binary data is transmitted over a telephone line with usable bandwidth of 2400 Hz using the FSK signaling scheme. The transmit frequencies are 2025 and 2225 Hz, and the data rate is 300 bits/Sec. The average signal to noise power ratio at the output of the channel is 6dB. Calculate Pe for the coherent and non coherent demodulation schemes..

3.a) Explain about coherent binary PSK transmitter and receiver. Assuming channel noise to be additive white Gaussian obtain expression for probability of error.

b) Calculate the transfer function of the Optimum filter.

4.(a)What is correlator

(b) Explain the optimum filter reception using correlator.

5(a)What is a matched filter? How it differs from a optimum filter.

(b)Derive an expression for impulse response of the matched filter.

6.Explain how integrator is used to detect the baseband signal. Obtain an expression for S/N of integrator and dump receiver.

UNIT IV: INFORMATION THEORY

1. a). Define entropy.

b). A source x generates four messages mo,m1, m2, m4 with probabilities 1/3, 1/6, 1/4, ¼ respectively. The successive messages emitted by the source are statistically independent. Calculate entropy of the source X.

2. a) Define and explain the following. i) Information ii) Efficiency of coding iii) Redundancy of coding.
   b) Prove that H(X,Y) = H(X) + H(Y/X) = H(Y) + H(X/Y).

3. a) State and prove the condition for entropy to be maximum.
   b) Prove that H(Y/X) ≤ H(Y) with equality if and only if X and Y are independent.

4.(a) What is mutual information? State and prove the properties of it.

(b) If I(x1) is the information carried by symbol x1 and I(x2) id the information carried by symbol x2 then prove that the amount of information carried compositely due to x1and x2 is I(x1, x2)= I(x1) I(x2)

5 An analog signal band limited to 10HKz quantize is 8-lavels of PCM System with probability of 1/4,1/5,1/4,1/10,1/20,1/10,1/20 and 1/10 respectively. Find the entropy and rate of information.

6 a) Explain the concept of amount of information. [8M]

b) An analog signal is band limited to B Hz, sampled at the nyquist rate, and the samples are quantized into 4 levels. The quantization levels Q1, Q2, Q3 and Q4 (messages) are assumed independent and occur with probabilities p1= p4=1/8 and p2= p3=3/8. Find the information rate of the source.

UNIT V :SOURCE CODING

1 Explain the Huffman coding technique with example.

2 a) Explain procedure of Shannon-fano coding and Huffman coding. b) A discrete memory less source X has 5 symbols x1, x2 x3, x4 & x5 with P(x1)=0.4, P(x2)=0.19, P(x3)=0.16, P(x4)=0.15 & p(x5)=0.1. (i) Construct a Shannon-fano code for X, and calculate the efficiency of the code. (ii) Repeat for the Huffman code and compare the results.

3 (a)Discuss the channel capacity for discrete and analog channels.

(b)Apply Shannon Fano coding for the 5 messages with probabilities 0.4, 0.15, 0.15, 0.15, 0.15 and find the coding efficiency.

4.What is binary symmetric channel and derive expression for its capacity.

5.A discrete memory less source has an alphabet of seven symbols with probability for its output, as described here:

Symbol	prob.
S_0	0.25
S_1	0.25
S_2	0.125
S_3	0.125
S_4	0.125
S_5	0.0625
S_6	0.0625

(i) Compute the Huffman code for this source and explain why the compute source code has an efficiency of 100 percent. (ii) Calculate H

UNIT VI :LINEAR BLOCK CODES&CONVOLUTION CODES

1.Define the linear block codes and explain matrix description of a linear block codes.
(b) The generator matrix for a (6, 3) block code is given below. Find all code vectors of this code. G= [I : P]; where P= [0 1 1; 1 0 1; 1 1 0], & I = Identity Matrix.

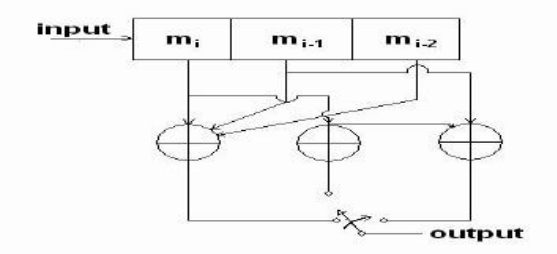
2.a) Explain the advantages and disadvantages of cyclic codes.

b) Construct the (7, 4) linear code word for the generator polynomial G(D) = 1+D2+D3 for the message bits 1001 and find the checksum for the same.

3.a) Explain the principle and operation of encoder for Hamming code.
b) An error control code has the following parity check matrix. *H* = [1 0 1 1 0 0; 1 1 0 0 1 0; 0 1 1 0 0 1] i) Determine the generator matrix 'G' ii) Decode the received code word 110110. Comment on error detection capability of this code.

4.A) State and explain the properties of cyclic codes.
b) The generator polynomial of a (7, 4) cyclic code is x3+x+1. Construct the generator matrix for a systematic cyclic code and find the code word for the message (1101) using the generated matrix.

5.a) Briefly describe the Viterbi algorithm for maximum-likelihood decoding of convolutional codes.
b) For the convolutional encoder shown in figure 1, draw the state diagram and the trellis diagram.



6 (a) What are code tree, trellis and state diagrams for a convolutional encoder?

(b) Draw the trellis diagram of a Convolutional code of code rate r=1/2 and Constraint length of K=3 starting from the state table and state diagram for an encoder which is commonly used.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL IC APPLICATIONS

Academic Year	: 2018-2019
Name of the Faculty	: B. NEELIMA DEVI
Designation	: ASST.PROFESSOR
Department	: ECE
Year/Semester	: III YEAR– I SEMESTER
Regulation	: R16
Subject	: DIGITAL IC APPLICATIONS

UNIT 1 - Digital Logic Families and Interfacing

1. (a) Discuss the behaviour of a CMOS as an inverter.i) Inductive effects ii) Propagation delay[5M]
   (b) What are features of TTL logic family? Discuss about the fastest logic family and mention the typical values of its various parameters.[5M]
2. (a)Draw the circuit diagram of basic TTL NAND gate and explain with the help of functional operation.[5M]
   (b) What are the advantages and disadvantages of ECL gates? Draw and explain the 2-input OR/NOR gate using ECL logic.[5M]
3. (a)Explain dynamic electrical behavior of a CMOS. [5M]
   (b) Design a 4 input CMOS AND-OR-INVERT gate. Explain the circuit with the help of logic diagram and function table.[5M]
4. (a) Explain the CMOS circuit behavior with resistive load. [5M]
   (b) Describe the key benefit of schottky transistors in TTL. [3M]
   (c) Explain about CMOS steady state electrical behavior. [2M]
5. (a) Explain about CMOS/TTL interfacing.[5M]
   (b) Draw a two input 10K ECL OR gate and verify the truth table. [5M]
6. (a) Explain the circuit behavior of CMOS with non ideal outputs. [5M]
   (b) Design 2-input LS-TTL NAND gate and explain its operation. Give the function table, truth table.[5M]
7. (a) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, propagation delay and fan-out.[8M]
   (b) Write about the totem pole arrangement in case of TTL family. [8M]
8. (a) Differentiate between the TTL and DTL logic families.[4M]
   (b) Discuss about dynamic electrical behavior. [4 M]
   (c) Draw the schematic diagram of a tri-state buffer and explain its operation. [2M]

UNIT-II- Introduction to VHDL

1. (a) What are the different data objects supported by VHDL? Explain scalar types with suitable examples.[5M]

(b) Write a VHDL Entity and Architecture for the following function.F = a (XOR) b (XOR)c, Also draw the relevant logic diagram.[5M]

2. (a) Write short note on package declaration. [2M]
   (b) Write a syntax of VHDL array declaration. [2M]
   (c) What statement is primarily used to describe a design in dataflow style? Explain about dataflow design elements of VHDL. [6M]
3. (a) What is the purpose of the 'timescale' compiler derivative? Give an example. [6 M]
   (b) Write a short note on Elements of VHDL. [2M]
   (c) Write short notes on sub programs.[2M]
4. What is the use of packages and libraries in VHDL? Explain with examples.[10M]
5. (a) Explain the terms entity, is, port, in, out and end pertaining to VHDL complier.Write a VHDL program using all the above terms and explain the same.[5M]
   (b) Write the features VHDL. [3M]
   (c) What are the comparison of VHDL and Verilog HDL[2M]
6. (a) Write VHDL Code of 8 x 1Mux using data flow. [5M]
   (b) Write a VHDL code for a 4 bit counter using behavioral modeling.[5M]
7. (a)Explain about Levels of Abstraction. [2M]
   (b)Write a VHDL code for a full adder using two half adders in structural modeling. [6M]
   (c) Brief the objects in VHDL.[2M]

UNIT-III- Behavioral Modeling

1. (a) With Example explain Process statement, variable assignment statement, signal assignment statement [6M]
   (b) Explain Transport Delay Model [4M]
2. (a) With Example explain wait statement and if statement [4M]
   (b) Write a short note on signal drivers [3M]
   (c) With Example explain case statement [3M]
3. (a) With Example explain null statement, loop statement, exit statement, next statement ,assertion Statement [6M]
   (b) Explain Multiple Processes concept with example. [4M]
4. (a) Explain Inertial Delay Model [5M]
   (b) Explain Other Sequential Statements [5M]
5. (a) How to Create Signal Waveforms [5M]
6. (a) Explain Logic Synthesis [5M]
   (b) Write a short note on Inside a logic Synthesizer. [5M]

UNIT-IV-Combinational Logic Design

1. (a) Write a VHDL code for a 4 bit up counter [4M]
   (b) Draw the truth table and circuit diagram of a 2-to-4 decoder. [4M]
   (c) Discuss about the implementation of comparator using digital IC. [8M]
2. (a) Explain about the Dual Priority Encoder with neat diagram.[8M]
   (b) Write a VHDL code to simulate a full adder circuit. [4M]
   (c) What is a floating point encoder? explain [4M]
3. (a) Design a full adder using two half adders. Write its structural code. [4M]
   (b) Design the logic circuit and write a data-flow style VHDL program for the following functions $F(X) = \Sigma A,B,C,D(0,1,3,5,14) + d(8,15)$ [8M]
4. (a) Write a data-flow style VHDL program for 4:1 MUX.[3 M]
   (b) Explain the working of carry look ahead adder and its advantages.[7 M]
5. (a) Design a 8bit ALU using two 74LS181 ICs.[8 M]

(b) Write VHDL code for half subtractor using structural modeling. [2 M]

6. (a) Write a VHDL program for8X3 encoder. [2 M]
   (b) Write VHDL code for 16 bit barrel shift. [3M]
   (c) Implement the 32 input to 5 output priority encoder using four 74LS148 gates. [5M]

UNIT-V-Sequential Logic Design

1. (a) Write a VHDL program to design a modulo-8 counter. [5M]
   (b) Write a VHDL program to simulate the behaviour of a positive edge triggered J-K flip – flop.[5M]
2. (a) Explain in detail about the working of Johnson Counter using 74 LS194. [5M]
   (b) Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style.[5M]
3. (a) Write a VHDL code for a 4 bit down counter. [2M]
   (b) Design a 8 bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.[5M]
   (c) Write a VHDL code for Ring counter. [3M]
4. (a) Design, explain and write VHDL code for Universal Shift Register. [8 M]
   (b) Write VHDL code for T Flip Flop with asynchronous reset using behavioural modelling.[2M]
5. (a) Design a 3 bit LFSR with an initial state of 6. [8M]
   (b) Design a modulo 11 counter using 74x163. [8M]
6. (a) Write the differences between flip-flop and latch. [2M]
   (b) Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using IC 74LS194.[5M]
   (c) Explain the different Modes of Operation of Shift Registers. [3M]
7. (a) Design a 4 bit synchronous binary even counter and write its behavioural model. [5M]
   (b) Discuss the steps involved in the analysis of sequential circuits. [2M]
   (c) Write a VHDL program to simulate the behavior of a positive edge triggered ‘D’flip – flop.[3M]

UNIT-VI- Synchronous and Asynchronous Sequential Circuits

1. (a)Draw state diagrams of a sequence detector which can detect 011 [3M]
   (b) Distinguish between Moore and Mealy Machines.[2M]
   (c) The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x2 changes from 0 to 1 while x1=1. The output changes from 1 to 0 only when x1 changes from 1 to 0 while x2=1. Find a minimum row reduced flow table [6M]
2. (a) Draw the diagram of Mealy type FSM for serial adder. [2M]
   (b) Explain the procedure of Meelay to Moore conversion [2M]
   (c) A clocked sequential circuit is provided with a single input x and single output z, whenever the input produces a string pulsed 111 or 000 and at the end of the sequence it produces an output z=1 and overlapping is also allowed. [6M]
   i) Obtain state diagram and state table.
   ii) Find equivalence classes using partition method and design the circuit using D flip- flop.

3. (a)Draw the state diagram of mod-8 Up - Down counter in Moore model and obtain its state table.
   (b) Explain the procedure of Meelay to Moore conversion
   (c) A clock mode sequential circuit has to provide z=1 whenever the input completes the Sequence of pulses 1010 and overlapping is allowed. Draw the state diagram and obtain minimal state using partition method

4. (a)Explain about sequential circuits, state table and state diagram.
   (b)Write capabilities and limitations of Finite- State machine.

(c)A sequential circuit has 2 inputs w1=w2 and an output z. It's function is to compare the i/p sequence on the two i/p's. If w1=w2 during any four consecutive clock cycles, the circuit produces, z = 1 otherwise z = 0, w1= 0110111000110, w2= 1110101000111, z=0000100001110.

5. (a) Define the state equivalence and machine equivalence with reference to sequential machines.
(b)Derive a circuit that realizes the FSM defined by the state assigned table below using JK flip flops

PS	NS, Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

(or)

Convert the following Mealy machine into a corresponding Moore machine? (10M)

PS	NS, Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

6. A clocked sequential circuit is defined by the following state table:
a) Using implementation table obtain equivalence classes.
b) Design the circuit using D-flip-flop.

P.S	NS, Z		Z	
	x = 0	x = 1	x = 0	x = 1
0	0	4	1	0
1	0	4	0	0
2	1	5	0	0
3	1	5	0	0
4	2	6	0	1
5	2	6	0	1
6	3	7	0	1
7	3	7	0	1

(or)

Find the equivalence partition and a corresponding reduced machine in a standard form for a given machine

PS	NS	Z
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

.

7. Convert the following Mealy machine into a corresponding Moore Machine.

8. PS	9. NS	a. Z
	10. X=0	11. X=1
12. A	13. C,0	14. B,0
15. B	16. A,1	17. D,0
18. C	19. B,1	20. A,1
21. D	22. D,1	23. C,0

b) Convert the following Moore machine into a corresponding Melay Machine

24. PS	i. NEXT STATE		25. OUTPUT 26. Z
	27. X=0	28. X=1	
29. A	30. D	31. B	32. 0
33. B	34. B	35. C	36. 1
37. C	38. C	39. D	40. 0
41. D	42. D	43. B	44. 0

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QUESTION BANK

COMPUTER ACHITECTURE AND ORGANIZATION

Class – III ECE – I Sem **Name of the Faculty- K. Nuka Raju**

UNIT –I

1) a) Explain the Functional unit of a computer - 5 M
   b) Explain the Basic Operational concepts of a Computer - 5 M
2) a) Explain about Bus structures -5 M
   b) Explain about the System Software. - 5 M
3) a) How to calculate the Performance of a computer Explain. - 5 M
   b) Explain the history of computer development. - 5 M
4) a) Explain the Functional unit of a computer - 5 M
   b) Explain about Bus structures - 5 M
5) a) Explain about the System Software. - 5 M
   b) How to calculate the Performance of a computer Explain. - 5 M

UNIT –II

1) a) Explain about the Register Transfer Notation - 5 M
   b) Explain about Assembly Language Notation - 5 M
2) a) Explain the Basic Instruction Types - 5 M
   b) Explain the different Addressing Modes -5 M
3) a) Explain about Basic Input/output Operations - 5 M
   b) Explain the role of Stacks and Queues in computer programming equation - 5 M
4) a) Explain about Logic Instructions - 5 M
   b) Explain about shift and Rotate Instructions - 5 M
5) a) Explain the Basic Instruction Types - 5 M
   b) Explain the role of Stacks and Queues in computer programming equation - 5 M

UNIT –III

1) a) Explain about Arithmetic Instructions. - 5 M
   b) Explain about Logic Instructions. - 5 M
2) a) Explain about Branch Instructions. - 5 M
   b) Explain about Different Addressing modes - 5 M
3) a) Explain about Diff input output operations - 5 M
   b) Explain about Different Addressing modes - 5 M
4) a) Explain about Arithmetic Instructions. - 5 M
   b) Explain about Branch Instructions. - 5 M

5) a) Explain about Logic Instructions. - 5 M
b) Explain about Different Addressing modes. - 5 M

UNIT –IV

1) a) Explain about Accessing I/O Devices - 5 M
b) Explain about Interrupt Hardware - 5 M
2) a) How do you Enabling and Disabling Interrupts - 5 M
b) How do you handle Multiple Devices - 5 M
3) a) Explain about Direct Memory Access - 5 M
b) Explain about Synchronous Bus - 5 M
4) a) Explain about Asynchronous Bus - 5 M
b) Explain about Interface Circuits - 5 M
5) a) Explain about Peripheral Component Interconnect (PCI) Bus - 5 M
b) Explain about Universal Serial Bus (USB) - 5 M

UNIT –V

1) a) Explain about Basic memory circuits - 5 M
b) Explain about Memory System Consideration - 5 M
2) a) Explain about ROM - 5 M
b) Explain about PROM - 5 M
3) a) Explain about EPROM - 5 M
b) Explain about EEPROM - 5 M
4) a) Explain about Flash Memory - 5 M
b) Explain about Mapping Functions - 5 M
5) a) Explain about Magnetic Hard Disks - 5 M
b) Explain about Optical Disks - 5 M

UNIT –VI

1) a) Explain about Register Transfers - 5 M
b) How to Perform Arithmetic Operations? Explain. - 5 M
2) a) How to Perform Logic Operations ?Explain. - 5 M
b) How to Fetch A Word From Memory? Explain. - 5 M
3) a) Explain Execution of Complete Instruction - 5 M
b) Explain about Hardwired Control - 5 M
4) a) Explain about Microinstructions - 5 M
b) Explain about Micro program Sequencing - 5 M
5) a) Wide Branch Addressing Microinstructions with next –Address Field - 5 M
b) Explain about Microinstructions - 5 M

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LINEAR IC APPLICATIONS

Academic Year : 2018-2019
Name of the Faculty : K. Archana
Designation : ASST.PROFESSOR
Department : ECE
Year/Semester : III YEAR– I SEMESTER
Subject : LINEAR IC APPLICATIONS

UNIT I - INTEGRATED CIRCUITS

1a) Define differential amplifier and draw its block diagram. [3M]
Derive the AC analysis of Single Input Dual Output Configuration in detail.
(or)
Derive the AC analysis of Dual Input Single Output Configuration in detail.
(or)
b) Derive the AC analysis of Dual Input Dual Output Configuration in detail. [7M]
(or)
Derive the AC analysis of Single Input Single Output Configuration in detail.

2a) Explain the operation of differential amplifier with swamping resistors [7M]
b) Why level translator is used with cascaded differential amplifier. [3M]
3a) Explain the methods of realizing high input resistance. [5M]
b) Explain the Properties of other differential amplifier configuration in detail. [5M]
4a) Derive the Differential Amplifier- DC analysis of Dual input Balanced output Configuration in detail. [5M]
b) Design 4 stage Cascade Differential Amplifier Stages and explain why cascading is required. [5M]
5a) Briefly explain about FET differential amplifier and calculate gain [3M]
b) Discuss the effect of R_E to improve CMRR and what are the methods to improve CMRR. [7M]

6.a) Explain the difference between constant current source and current mirror. [7 M]

b)Why level translator is called emitter follower [3 M]

(or)

Explain why level translator is called voltage follower

UNIT II- Characteristics of OP-Amps (IC 741)

1a) Explain the terms (i) slew rates (ii) CMRR (iii) PSRR (iv) drift and List out ideal and practical characteristics of above parameters [7M]

b) An Op-Amp has a slew rate of 2V/μ sec. What is the maximum frequency of an output signal of peak value 5V at which the distortion sets in due to the slew rate limitation? [3M]

2a) Explain stability of an Op-amp and ideal voltage transfer curve of an Op-amp [3M]

b) Explain the operation of Op-amp along with block diagram in detail. [7M]

3a) Explain the Frequency Compensation techniques of op-amp in detail. [5M]

b) Draw the IC 741 op-amp pin diagram and explain the function of each pin in detail. [5M]

4a) Listout DC and AC characteristics of opamp and Explain the terms Input & Out put Off set voltages & currents. [5M]

b) List out the applications and Temperature ranges of IC 741 Op-amp. [5M]

5a) Explain different Package Types of op-amps. [3M]

b) (i)Explain open loop configurations of CMRR. [3M]

(ii)Explain the basic processes used in silicon planer technology with neat diagram. [4M]

[7M

6. Write a brief note on [Each 2 ½ M]

(a) Photo lithography

(b) Photo etching

(c) Epitaxial growth

(d) Diffusion

7. (a) Explain how the input offset voltage compensated for. [3 M]

(b) Why FET op-amps are better than BJT Op-amps? [3 M]

(c) Explain the term slew rate and how it affects the frequency response of op-amp? [4M]

8. (a) Explain different IC packages. Mention the criteria for selecting an IC package and give different scales of integration. [5M]

(b)What do you mean by the term virtual ground? [2M]

(c)Explain the use of active load to improve CMRR .[3M]

9. Explain the following compensation techniques [Each 2 M]

(a) Frequency compensation

(b) External compensation

(c) Internal compensation

(d) Dominant pole compensation

(e) Pole-Zero compensation

UNIT III- LINEAR & NON-LINEAR APPLICATIONS OF OP- AMPS

1a) Draw the non inverting op-amp circuit diagram and derive its output voltage. [3M]

b) Draw the circuit diagram of differentiator &integrator by using IC 741 and explain its operation. [3M]

c) Explain the summer and difference amplifier using IC 741 and explain its operation. [4M]

2a) Draw and explain Op amp Schmitt trigger. [4M]

b) Draw the block diagram of log Amplifiers and explain its operation in detail. [6M]

3a) What are the limitations of log amplifier and how to overcome those limitations explain in detail. [4M]

b) Draw the precision half wave rectifier, V to I and I to V convertor circuit diagram and explain briefly. [3M]

c) Define virtual ground and Prove inverting Op amp gain is $-\frac{Rf}{R1}$. [2M]

4a) Explain the operation of Square wave generators along with circuit diagram. [5M]

b) Draw the block diagram of Non- Linear function generation and explain its operation. [5M]

5a) Draw the Instrumentation amplifier and explain its operation in detail. [5M]
Draw the Anti log Amplifiers circuit diagram and derive its output voltage in detail.

6a) Explain how to obtain triangular wave using square wave. [6 M]

(or)

Explain how to obtain triangular wave using integrator

(or)

Explain how to obtain triangular wave using schmitt trigger

b)What is the main advantage of comparator based triangular wave generator over free running astable multivibrator based circuit?. [4 M]

7 (a) Explain practical integrator by showing initial conditions. [5 M]

b) Distinguish comparator with Schmitt trigger. [5 M]

8 (a) Explain hysteresis curve in Schmitt trigger. [5 M]

(b) Explain 3 op-amp instrumentation amplifier [5 M]

9 (a) Explain the operation of AC inverting amplifier [5 M]

(b)Explain asymmetric square wave generator. [5 M]

10 a) Explain linear ramp generator [5 M]

b) Explain V to I converter with floating load . [5 M]

UNIT IV
ACTIVE FILTERS, ANALOG MULTIPLIERS AND MODULATORS

1a) Explain the operation of $1^{st}/2^{nd}/3^{rd}$ order butterworth LP with upper cutoff frequency 1Khz [5M]

b) Explain the operation of $2^{nd}/3^{rd}/4^{th}$ order band reject filter along with circuit diagram. [5M]

2a) Define filters and Draw the frequency response and explain characteristics of HPF, BPF, BRF and APF. [5M]

b) Draw the block diagram of Four Quadrant multiplier and explain its operation in detail. [5M]

3a) Design a second order low-pass Butterworth filter with a cut-off frequency of 12 KHz and unity gain at low frequency. Also determine the voltage transfer function magnitude in dB at 15Hz for the filter. (Draw second order butterworth high pass filter also draw its frequency response) [5M]

b) List out the applications of analog switches. [2 M]

c) Explain twin T notch filter [3M]

4a) Draw the block diagram of balanced modulator and explain its operation in detail and List out the features of IC 1496 balanced modulator . [7M]

b) Design a wide band filter f_h=400Hz , f_l=2Khz, having the passband gain 2. [3M]

5a) Draw the circuit diagram of Sample & Hold amplifier and explain its operation in detail. [5M]

b) Draw the circuit diagram of All pass filters and write its output voltage equation.derive its output response. [5M]

UNIT V- TIMERS & PHASE LOCKED LOOPS

1a) Draw the pin diagram of IC 555 and explain each pin. [3M]

b) Draw and Explain the principles and description of individual blocks of PLL in detail. Also discuss the applications of PLL in phase detector and VCO [7M]

2a) Explain the terms frequency multiplication, frequency translation, tracking range and capture range of PLL. [5M]

b) Give functional block diagram of VCO NE 565 and explain its working and necessary expression for free running or center frequency. [5M]

3a) Draw the circuit diagram of FSK demodulators and explain its operation in detail. [5M]

b) Draw the block diagram of Astable operations (free running) using IC 555 and derive its time constant. [5M]

Or

Draw the circuit diagram of Monostable multivibrator by using IC 555 timer and explain its operation and derive the expression of time delay.

4a) Draw the circuit diagram of VCO 566 and explain its operation with any example. [6M]

b) Discuss the role phase detector in PLL and explain thedigital phase detector used in it. [4M]

5a) Drawthe block diagram of Astable operations (free running) using OP-amp and explain its working. [5M]

b) What are the modes of operations of 555 timer and explain the working of Schmitt trigger using 555 timer? [2M]

c) Derive the expression for capture range for PLL where a single RC network is used as a LPF. [3M]

UNIT VI
DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS

1a)	List out different ADCs and justify which A/D convertor is best in terms of speed.	[3M]
b)	Draw the block diagram of inverted R-2R DAC and explain its operation in detail.	[7M]
2a)	List out the DAC and ADC Specifications and compare them in detail.	[6M]
b)	Define the terms Linearity, resolution, settling time and accuracy of A/D convertors.	[4M]
3a)	An 8 bit ADC outputs all is when V_i=5.1v. Find resolution and digital output when V_i=1.28v.	[5M]
b)	Draw the circuit diagram of weighted resistor DAC and explain its operation in detail.	[5M]
4a)	What are the basic DAC techniques?	[3M]
b)	Draw the block diagram of successive approximation ADC and explain its operation in detail. Or Draw the circuit diagram of counter type ADC and explain its operation in detail Or Draw the block diagram of parallel Comparator type ADC and explain the operation of it Explain its operation with waveforms. What parameters decide its conversion speed and accuracy?	[7M]
5a)	Draw the block diagram of dual slope ADC and explain its operation in detail.	[5M]
b)	Or Draw the circuit diagram of dual slope integration AD converter and state its advantages.	[5M]
6a)	What are the basic blocks preceding an ADC in a typical application like digital audio recording?	[5M]
b)	What are the different sources of errors in DAC? Explain.	[5M]

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NH-5, Anakapalle – 531002, Visakhapatnam, A.P.

Phone: 08924-221111 / 221122/9963981111, www.diet.edu.in, E-mail: info@diet.edu.in

Academic Year : 2018-2019
Name of the Faculty : MOHAMMAD SHAFFI
Designation : Asst. Professor
Department : ECE
Year/Semester : III –I Semester
Subject : PULSE and DIGITAL CIRCUITS

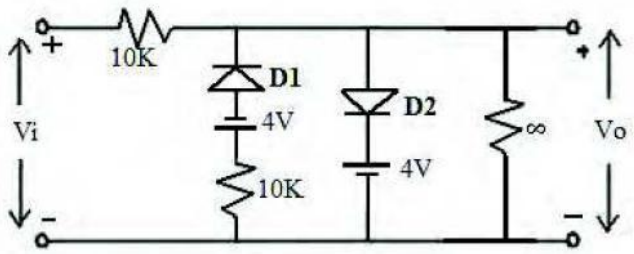
QUESTION BANK

UNIT-I

1. a) Prove that a low pass circuit acts as an integrator. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input.(5M)
   b) Explain RLC ringing circuit with a neat sketch.(5M)
2. a) Draw the output waveform of an RC high-pass circuit with a square wave input under different time constants. Derive the expression for percentage of tilt. (5M)
   b) What is an attenuator? How can an uncompensated attenuator be modified as a compensated attenuator. Give the comparison between perfect compensation, under compensation and over compensation. (5M)
3. a) Derive an expression for the output of low pass RC circuit excited by a step input.Draw the output for different time constants.(5M)
   b) Draw the response of an RC high pass circuit when applied with exponential input. Explain the response for different time constants. (5M)
4. a) An RC low-pass filter is fed with a symmetrical square wave. The peak-to-peak amplitude of the input waveform is 10 V and its average value is zero. It is given that RC=*T/2* where *T* is the period of the square wave. Determine the peak-to-peak amplitude of the output waveform. (5M)
   b) Prove that et = T/2RC for ramp as input to the High pass RC-Circuit? (5M)
5. a) Explain the working principle of rate-of-rise amplifier? (5M)
   b) Explain the working of attenuator as a CRO Probe? (5M)

UNIT-II

1. a) Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics .(5M)
   b) State and prove clamping circuit theorem.(5M)
2. a) Write short notes on practical clamping circuits. (5M)
   b) A voltage signal of (10 Sinwt) is applied to the circuit with ideal diodes shown in figure below. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation.(5M)



3. a)Draw the basic circuit diagram of negative peak clamper circuit and explain its Operation.
   b) Give some applications of clipping & Clamping circuits. (5M)
4. a) With neat circuit diagram, explain the working of an emitter coupled clipper. (5M)
   b) Explain the clamping circuit considering the source resistance and the diode forward resistance. (5M)
5. a) A symmetrical 50 Hz square wave whose peak to peak excursions are ± 100 V with respect to ground is to be positively clamped at 25 V. Draw the necessary circuit diagram and output waveform for this purpose. (5M)
   b) Design a diode clamper to restore the negative peaks of the input signal to zero level. Use a silicon diode with R_f= 50 Ω and R_r= 400 kΩ. The frequency of the input signal is 5 kHz.(5M)

UNIT –III

1. Explain the terms pertaining to transistor switching characteristics.
   i) Rise time.[2M] ii) Delay time. [2M] iii) Turn-on time.[1M]
   iv) Storage time.[2M] v) Fall time.[2M] vi) Turn-off time.[1M]
2. a) Describe the sequence of events in an n-p-n transistor to change from cutoff to saturation and vice versa. How does temperature affect the saturation junction of a transistor? (5M)
   b) Briefly discuss the influence of breakdown voltages on the choice of supply voltage in a transistor switch. (5M)
3. a) Design a Schmitt trigger circuit using npn silicon transistors with V_{BE} = 0.7V, $V_{CE(sat)}$ = 0.2V, $h_{fe(min)}$ = 60 and $I_{c(ON)}$= 3mA to meet the following specifications: V_{cc} =12V, upper threshold voltage, V_{UT}= 4V, lower threshold voltage,V_{LT}=2V. (5M)
   b) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary. (5M)
4. a) With neat circuit diagram, Explain the working of fixed bias bistable multi vibrator. (5M)
   b) Calculate the component values of a mono stable multi vibrator developing an output pulse of 500 μs duration. Assume $h_{fe(min)}$ = 25, $I_{CE(min)}$= 5 mA, V_{CC}= 10 V and V_{BB} = -4V. (5M)
5. a) Draw the circuit of a bistable multivibrator with symmetrical collector triggering. (5M)
   b)What are commutating capacitors? Show a symmetrical triggering arrangement for bi-stable multivibrator and explain its working. (5M)

UNIT -IV

1. a) Explain the operation of a Monostable multivibrator and derive for the pulse width with necessary waveforms & circuirts. (5M)
   b) Design a collector coupled astable multivibrator using NPN silicon transistors with h_{fe}=40, r_{bb}=200ohms supploied with V_{cc}=10V and circuit component values are R_c=1.2Kohms and C=270 pF. (5M)

2. a) Draw the circuit diagram of an astable multivibrator and obtain all the steady state voltages and currents. Show how it acts as a voltage to frequency converter. (5M)

b) Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with $h_{FE(MIN)}$ =20. In stable state, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the $I_{B(MIN)}$ value. Assume V_{CC} = 8V, $I_{C(SAT)}$ =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R_1, C and V_{BB} . (5M)

3. a) Design a stable multi vibrator to generate a square wave of 1 kHz frequency with a duty cycle of 25% using silicon n-p-n transistors with $h_{FE(MIN)}$ = 40. (5M)

b) Design a collector coupled one-shot with a gate width of 3 ms using NPN transistors Assume necessary data. (5M)

4. Explain the operation of a Monostable multivibrator and derive for the pulse width with necessary waveforms & circuirts.[10M]

5. a) Derive the equation for voltage-to-frequency converter when a stable multi vibrator is used as a basic circuit. (5M)

b) The Schmitt trigger circuit also called sinusoidal to square converter? Explain the working principle. (5M)

UNIT -V

1. Explain the working of a transistor Bootstrap sweep circuit and derive expression for the slope sweep error. (10M)
2. a) Why the time base generators are called sweep circuits? Give most important applications of time –base generators. (5M)
   b) What are the different methods of generating time-base waveforms? Explain about each briefly. (5M)
3. Explain the working of Transistor Miller sweep circuit. What are its advantages over Bootstrap sweep circuits? (5M)
4. a) Define and derive the terms slope error, displacement error and transmission error. (5M)
   b) How is deviation of linearity expressed? What do you mean by sweep time and restoration time? (5M)
5. Explain the basic principles of Miller and Bootstrap time-base generators. Give the comparison of both the generation methods. (10M)

UNIT-VI

1. a) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. (5M)
   b) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram. (5M)
2. a) Explain the function of a sampling gate used in Sampling Scopes also explain how sampling gate is used in chopping amplifiers. (5M)
   b) Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate. (5M)
3. a) Explain about unidirectional diode sampling gate. Write its advantages and disadvantages. (5M)
   b) With neat circuit diagram, Explain bidirectional sampling gate using transistors. (5M)
4. a) What is meant by synchronization? Why it is needed? Explain. (5M)

b) Explain about four diode sampling gate. (5M)

5. a) Explain about phase delay and phase jitters. (5M)
   b) Explain how pedestal can be reduced in gate circuit. (5M)

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Phone: 08924-221111 / 221122/9963981111, www.diet.edu.in, E-mail: info@diet.edu.in

QUESTION BANK

Academic Year	:	2018-2019
Name of the Faculty	:	Mr. P. Ram Prasad
Designation	:	Assistant Professor
Department	:	Electronics & Communication Engineering
Year & Semester	:	III – I Semester
Regulation	:	R16
Subject	:	Antenna and Wave Propagation

UNIT-I

1. a) Sketch and comment on the current distributions and radiation patterns of vertical antennas of length l/2, l, 3l/2, 2l. [5M]
   b) Derive the relationship between effective aperture area and gain of antenna. [5M]
2. a) Define the terms: i) Effective length ii) Effective aperture area. [5M]
   b) Calculate effective length and effective aperture area of antenna whose radiation resistance is 73 ohms. [5M]
3. a) Define and explain the following terms: [5M]
   (i) Directivity (ii) Gain (iii) Aperture Efficiency
   b) An antenna has a radiation resistance of 72Ω, a loss resistance of 8Ω and a power gain of 12 dB. Determine the antenna efficiency and its directivity. [5M]
4. a) Explain the terms Isotropic, Directional, Omni directional patterns and Radiation intensity. [5M]
   b) Show that the radiation resistance of a λ/4 monopole is 36.5ohms. [5M]
5. a) Discuss the current distribution on a thin wire antenna. [5M]
   b) In a microwave communication link, two identical antennas operating at 10 GHz are used with power gain of 40 dB. If the transmitter power is 1W. Find the received power, if the range of the link is 30Km. [5M]

UNIT-II

1. a) Calculate the relative amplitudes of Radiation, Induction and Electrostatic Fields at a distance of 2λ from the short current element. [5M]
   b) Prove that if Power radiated (Pr) is expressed in terms of capacitance and voltage and if the voltage is held constant, that the radiated power will then proportional to the fourth power of frequency for a Hertzian Di-Pole. [5M]
2. a) The radiation intensity of a particular antenna is given by $Ø(\theta, Ø) = \sin^2\theta$. Calculate the directivity of the antenna. [5M]
   b) Show that the radiation resistance of a small loop is equal to $320\pi^4(A/\lambda^2)$ ohms where A is loop area. [5M]
3. a) Derive the expressions for electric field in case of short current element and hence obtain the conditions for the field to be in Franhofer region. [5M]
   b) Find the distance from a radiating element with 60Hz current such that radiation and induction fields are equal. [5M]
4. a) Show that the radiation resistance of half wave dipole is 73ohm. [5M]
   b) Distinguish between Dipole and Monopole. [5M]
5. a) Explain the concept of retarded scalar and vector potentials. [5M]
   b) Obtain expression for potential fields due to sinusoidally varying sources and bring out the importance of Lorentz guage condition. [5M]

UNIT-III

1. a) Explain the principle of pattern multiplication. What is the effect of earth on the radiation pattern of antennas. [5M]
   b) A uniform linear array consists of 16 isotropic point source with a spacing of λ/4 if the phase difference $\alpha=-90^0$. Find i. HPBW. ii. Directivity iii. Effective aperture [5M]
2. a) Compare the performance of Broadside and End fire array. [5M]
   b) Show that the width of principle lobe of an end fine array is greater than that of broadside array of the same length. [5M]
3. a) Show that directivity of a BSA of two identical isotropic in phase point sources Spaced a distance d=λ/2 is given by D = {2/[1 + 1/ßdsinßd]}. [5M]
   b) The radiation intensity $U=A_0\sin\theta$ for an antenna. Determine the directivity. [5M]
4. a) Derive the conditions for the linear array of N isotropic elements to radiate in end fire and find the first two side lobe levels. [5M]
   b) Prove that the level of secondary lobe is -13.5dB below that of major lobe in a uniform linearly array. [5M]
5. a) Briefly explain the following: [5M]
      i. Principle of pattern multiplication ii. Binomial array

b) A linear broadside array consists of four equal isotropic in phase point sources with λ/3 spacing & overall length of the array is λ. Find the directivity & beam width. [5M]

UNIT-IV

1. a) Distinguish between Traveling wave and Standing wave antennas. [3M]
   b) Compare Resonant and Non Resonant antennas. [3M]
   c) Explain the working of Rhombic antenna. [4M]
2. a) Describe the characteristics of long wire traveling wave antenna. Sketch their pattern for lengths of: i.λ/2 ii. 5 λ iii. 20 λ. [5M]
   b) With reference to paraboloides, Explain the following: [5M]
   (i)Aperture efficiency (ii)Front to back ratio (iii)Types of feeds
3. a) Explain the construction and radiation characteristics of Helical Antenna. [5M]
   b) Discuss how the directivity of horn antenna can be measured. [5M]
4. a) Explain the principle and working of Yagi Antenna. [5M]
   b) Design YagiUda antenna of six elements to provide a gain of 12dB if the operating frequency is 200MHz. [5M]
5. a) What is Zoning? What are its advantages? [5M]
   b) With neat setup, explain the absolute method of measuring the gain of an antenna. [5M]

UNIT-V

1. a) Describe the methods for measuring the below parameters for an antenna [5M]
   i) Gain ii) Directivity with a neat block diagram
   b) Distinguish between sectoral, pyramidal and conical horns, with neat sketches. List out their utility and applications. [5M]
2. a) List out the differences between active and passive corner reflectors. [5M]
   b) With reference to paraboloids, explain the following: [5M]
   i) f/D ratio ii) Spill over and aperture efficiency iii) Front to back ratio
3. a) Explain the principle of formation of images in an active corner reflector antenna. Hence sketch the image formation for a 90^o corner reflector. Obtain array factor for 90o corner reflector. [5M]
   b) What is the principle of equality of path length? How is it applicable to Horn antennas? Obtain an expression for the directivity of a pyramidal horn in terms of its aperture dimensions. [5M]
4. a) With neat set up, explain the absolute method of measuring the gain of an antenna. [5M]

b) Discuss about Dielectric and metal Lens Antennas and their applications. [5M]

5. a) Explain the Cassegrain and offset feed of Parabolic Antenna in detail. [5M]

b) How is the field pattern of a receiving antenna experimentally determined. Explain with a neat diagram. [5M]

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UNIT-VI

1. a) Describe briefly the salient features of ground wave propagation. [5M]

b) What should be the polarization of EM wave for the ground wave propagation? Justify. [5M]

2. a) Explain the term" wave tilt of surface waves". [5M]

b) List out the modes of propagation and their frequency ranges for radio waves. Show that the electric field strength of space wave propagation is given by $E = \frac{4\pi h_t h_r}{\lambda d^2} E_0$ [5M]

3. Write a short notes on: i) MUF ii) Virtual Height

iii) Skip Distance iv) Multihop Transmission. [10M]

4. a) Derive the relationship between MUF and critical frequency. [5M]

b) Show that the radius of curvature of ray path is given by $2/(d\varepsilon_r/dh)$ for tropospheric waves. 5M

5. a) Describe any two types of fading normally encountered in radio wave propagation. How are the problems of fading overcome? [5M]

b) Determine the change in the electron density of E-layer when the critical frequency changes from 4 MHz to 1 MHz between mid - day and sun-set. [5M]