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Code No: R31045

**R10**

**Set No: 1**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**ANTENNAS AND WAVE PROPAGATION**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Classify the field regions of an antenna? [5M]  
b) Prove that far field distance from the antenna is  $R \geq \lambda/6$  [10M]
2. a) Prove that the effective length of an antenna in transmitting mode is same as in receiving mode? [10M]  
b) What is the length of half-wave dipole at frequency 100 Hz, 10KHz and 10MHz.[5M]
3. Analyse and draw the radiation pattern of N-element array with spacing  $\lambda/2$ . [15M]
4. a) Explain the construction and working principle of inverted V- antenna placed on a ground? [10M]  
b) Calculate Radiation resistance and maximum direction of  $2\lambda$  long wire antenna?[5M]
5. Design and explain N- element circular loop yagi-uda antenna working at 3MHz? [15M]
6. a) Discuss different types of horn antennas? [8M]  
b) How to decide flared angle in horn antennas? [7M]
7. a) What is deadzone? Explain? [5M]  
b) Derive the equation for maximum usable frequency of skywave propagation in terms of incident angle and flat earth case? [10M]
8. a) Calculate LOS distance of Space wave propagation for flat earth with effective radius? [12M+3M]  
b) Define Radio Horizon?

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Set No: 2

JNT University Kakinada

III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**ANTENNAS AND WAVE PROPAGATION**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. Define the following  
i) Beam area ii) solid angle iii) Resolution iv) Radiation [15M]
2. a) what are antenna parameters? Explain? [10M]  
b) Find the efficiency, directivity and effective area of an antenna if its  $R_r=80\Omega$ ,  $R_l=10\Omega$ , power gain is 10dB and operating frequency is 100MHz. [5M]
3. Prove that SLR is constant in N-element array antenna with uniform distribution? [15M]
4. a) What is non-resonant antenna? Give the differences between resonant and non-resonant antenna? [7M]  
b) Design a Rhombic antenna to operate at a frequency of 30MHz, if the angle of elevation is  $40^\circ$ ? [8M]
5. a) Derive the input impedance of N-turn folded dipole antenna? [10M]  
b) Find the input impedance of 3-turn folded dipole antenna? [5M]
6. a) Derive the FRIIS Transmission formula? [10M]  
b) Find the basic transmission loss between a ground-based antenna and airborne antenna when the distance between the antennas are 320km at a frequency of 300MHz? [5M]
7. a) Briefly explain Modes of Propagation? [10M]  
b) Find out the relative permittivity of E-layer of the ionosphere with electron density is  $5 \times 10^5$  electrons/cm<sup>3</sup> and operating frequency 50MHz. [5M]
8. a) what is duct propagation? How it is better than spacewave propagation? [10M]  
b) Determine the radio horizon distance for a transmitting antenna height of 300feet? [5M]

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Code No: R31045

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Set No: 3

JNT University Kakinada

III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**ANTENNAS AND WAVE PROPAGATION**

(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. a) Show that the frequency of radiated field from antenna is same as source frequency ? [8M]  
b) Draw the current distribution on  $\lambda/10$ ,  $\lambda/4$ ,  $\lambda/2$ ,  $\lambda$  and  $2\lambda$ ? [7M]
2. Derive the field equations of small circular loop antenna and find  $R_{rad}$ ? [15M]
3. a) Prove that there are no sidelobes in binomial array antenna? [10M]  
b) A broad array contains 100 isotropic radiators with an inter element spacing of  $0.5 \lambda$ . Find the directivity? [5M]
4. Explain the construction and working principle of Helical Antenna in normal mode and axial mode? [15M]
5. a) Explain the working principle of cassegrain feed antenna? [8M]  
b) Discuss merits, demerits and applications of cassegrain feed antenna? [7M]
6. a) Explain need of Lens antennas? Explain types of Lens antennas? [10M]  
b) Find the bandwidth of zoned lens antenna if number of steps are 4 and refractive index 1.5? [5M]
7. A broadcast transmitter supplies 100KW to an antenna that radiates 50% of this power. The antenna has directional characteristic such that the field strength without ground losses is given by  $E_0=300 \times 1.28(P_{kw})^{1/2}$  mv/m at 1km. Find the field strength of the ground wave at 100km for the following conditions,  $f= 500\text{kHz}$ ,  $\epsilon_r=20$ ,  $\sigma=10^{-4}$  mho/cm. [15M]
8. a) Derive the field strength at LOS distance in spacewave propagation? [10M]  
b) Determine the radio horizon distance for a receiving antenna height of 150feet? [5M]

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Set No: 4

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**ANTENNAS AND WAVE PROPAGATION**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. Define the following  
i) Directivity ii) power gain iii) Principle plane iv) HPBW & FNBW [15M]
2. Prove that the quarter wave monopole  $R_{rad} = 36.5\Omega$ . [15M]
3. a) Define scanned array antenna? [7M]  
b) Explain the Hansen-woodyard Condition? [8M]
4. a) What is Grating lobe? How it can eliminate in array antenna? [8M]  
b) Explain working principle of V-antenna? [7M]
5. a) Find the field gain of a flatsheet reflector antenna? [8M]  
b) A parabolic reflector is required to have a power gain of 1,000 at a frequency of 3GHz. Determine the mouth diameter and beamwidth of the antenna? [7M]
6. a) Discuss the merits and demerits of antenna outdoor and indoor test? [8M]  
b) Find the gain of a test antenna using 3-Antenna technique? [7M]
7. a) Derive the cut of frequency of ionospheric layer? [10M]  
b) If the critical frequency of an ionized layer is 1.5MHz, find the electron density of the layer? [5M]
8. a) Explain space wave propagation? [7M]  
b) Determine the radio horizon distance for a transmitting antenna height of 300m and receiving antenna height of 150m? [8M]

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Code No: R31041

**R10**

**Set No: 1**

JNT University Kakinada

III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**COMPUTER ARCHITECTURE & ORGANIZATION**

(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Convert the following binary numbers to decimal and hexadecimal numbers  
1011011, 11101101, 1011011, 11001100  
b) Convert hexadecimal numbers to binary and octal numbers. FACDF, EEFFC, CF979, 79797
2. a) What is the differences between a direct and indirect addressing instructions? How many references to memory are needed for each type of instruction to bring an operand in to a process register?  
b) Draw circuit for one stage adder & logic unit and explain each block.
3. a) Discuss about the process organization in computer.  
b) Discuss about the register organization in computer.
4. a) Derive an algorithm in flowchart form for the nonrestoring method of fixed point binary division.  
b) Derive an algorithm for evaluating the square root of a binary fixed point number.
5. a) Draw the memory hierarchy in a computer system and explain each block.  
b) Discuss importance of cache memory organization.
6. a) What is the importance of interface module in computer system?  
b) What is the differences between isolated I/O and memory mapped I/O? What are advantages disadvantages of each?
7. a) Explain the advantages of symmetric multi processors over uniprocessors  
b) Discuss the various schemes to solve the cache coherence problem.
8. a) List the characteristics of multiprocessors.  
b) Draw the interconnection structures of computer systems.

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Code No: R31041

**R10**

**Set No: 2**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**COMPUTER ARCHITECTURE & ORGANIZATION**

(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Represent the number (+56.5) decimal as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8bits.  
b) Obtain 9's complement of the following 8 bit decimal number.  
12344321, 79797979, 89898989, 99999999
2. a) List out the instruction formats used in the processor and discuss with example.  
b) compare high & low level language with respect to execution time.
3. a) Define following terms, micro operations, microinstruction, micro program, micro code.  
b) Explain the differences between hardwired control and micro programmed control.
4. a) Draw the block diagram of 4 bit BCD adder and write operation.  
b) Explain about registers for floating point arithmetic operation.
5. (a) Discuss about the Address Translation in Virtual Memory in computer system.  
(b) Explain different types of mapping functions in cache memory.
6. a) Draw the block of a typical asynchronous communication interface and explain operation.  
b) List the modes of a transfer data to external devices and discuss operation.
7. a) Explain the pipe line process with timing of instructions.  
b) Explain the operation of RISC pipe line.
8. Brief the following
  - a. parallel arbitration
  - b. inter process arbitration

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JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015  
**COMPUTER ARCHITECTURE & ORGANIZATION**  
(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Perform the following arithmetic operations with the decimal numbers using signed 10's complement representation for negative numbers.  
i)  $(-666) + (+785)$  ii)  $(-638) + (+188)$   
b) Derive the circuits for a 3 bit parity generator and 4-bit parity checker using an even parity bit.
2. List out the basic computer hardware components and explain operation. Draw the flow chart for computer operation and discuss each block.
3. a) Draw the block diagram of microprogram control organization and explain.  
b) Discuss how selection of address for control memory.
4. a) Discuss about one stage of a decimal arithmetic unit.  
b) Discuss about adding of decimal numbers methods.
5. Explain about mapping function. What are different methods the cache can be mapped explain in detail.
6. a) Why does DMA have priority over the CPU when both request a memory transfer?  
b) Differentiate synchronous and asynchronous data transfer modes.
7. a) Discuss about multi threading.  
b) Discuss about vector computations.
8. Brief the following  
(a) Time shared common bus  
(b) inter process arbitration

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Set No: 4

JNT University Kakinada

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**COMPUTER ARCHITECTURE & ORGANIZATION**

(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. a) Show the bit configuration of a 24 bit register when its content represents the decimal equivalent of 280 i) in binary ii) in BCD iii) in ASCII using eight bits with even parity  
b) Explain the components of the Computer system.
2. a) Explain about machine instruction characteristics  
b) Explain about addressing modes operation and what is the importance of it.
3. a) Discuss about pipeline process system.  
b) Draw the circuit for status register bits and explain.
4. a) Show that there can be no mantissa overflow after a multiplication operation.  
b) Derive an algorithm in flow chart form for the comparison of two signed binary Numbers when negative numbers are in signed 2's complement representation
  - (i) By means of a subtraction operation with the signed 2's complement numbers.
  - (ii) By scanning and comparing pairs of bits from left to right.
5. a) i) How 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes.  
ii) How many lines of the address bus must be used to access 2048 bytes of memory. How many other lines will be common to all chips.  
iii) How many lines must be decoded for chip select ?specify the size of the decoders.  
b) Discuss about auxiliary memory devices.
6. a) List the importance of handshaking in data transfer operations.  
b) Discuss about serial communication system.
7. a) What are sub operations performed in arithmetic pipeline .  
b) Explain about pipe line process organization.
8. Brief the following
  - (a) inter process communication
  - (b) inter process synchronization

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Code No: R31046

**R10**

**Set No: 1**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL COMMUNICATIONS**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Explain the PCM technique and evaluate the expression for SNR in PCM.  
(b) 24 Telephone channels, each band limited to 3.4 KHz, are to be time division multiplexed by using PCM. Calculate the bandwidth of the PCM system for 128 quantization level and an 8 KHz sampling frequency.
2. (a) Explain the working of an adaptive delta modulation system with a discrete set of values for the step size with a neat block diagram.  
(b) Compare the noise performance in PCM and Delta modulation systems.
3. (a) What is continuous phase FSK? Explain the generation of continuous phase FSK signal.  
(b) Compare the noise performances of BASK, BFSK and BPSK for fixed average transmitted power and identical noise environment.
4. (a) Explain the non-coherent detection method of BFSK signaling.  
(b) Derive the expression for bit error probability of a QPSK receiver. Compare it with PSK receiver.
5. (a) Derive the expression for mutual information and describe its properties.  
(b) A message source generates one of four messages randomly every microsecond. The probabilities of these messages are 0.4, 0.3, 0.2 and 0.1. Each emitted message is independent of the other messages in the sequence. Determine the entropy and rate of information generated by the source.
6. (a) Derive the expression for the channel capacity of a discrete memoryless channel.  
(b) A discrete memoryless source has the letters A, B, C, D, E, F and G with corresponding probabilities {0.08, 0.2, 0.12, 0.15, 0.03, 0.02, 0.4}, design Huffman code for the above source and determine the average length of the codeword and coding efficiency.
7. (a) Draw the block diagram of an encoder for an (n, k) linear cyclic code and explain its working.  
(b) Taking  $x^3+x+1$  as the generator polynomial for the (7,4) cyclic linear block code, determine the code vectors in systematic form for the following message sequences:  
(i) 1011           (ii) 1111
8. (a) Explain the differences between the block codes and convolutional codes.  
(b) Explain tree diagram, trellis diagram and state transition diagram of convolutional codes with an example.

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Code No: R31046

**R10**

**Set No: 2**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL COMMUNICATIONS**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Derive expressions for the quantization noise and signal to noise ratio in a PCM system using uniform quantizer.  
(b) What is the need for companding in PCM? Draw the transfer characteristics of a companding system.
2. (a) Describe the principle of delta modulation with a relevant block diagram and waveforms.  
(b) Compare the Delta modulation and adaptive delta modulation systems.
3. (a) Explain the working of a differential PSK with the help of a neat block diagram.  
(b) Draw and explain the signal space diagram of QPSK and show the signal constellation.
4. (a) Derive the expression for probability of error for matched filter.  
(b) Describe the comparison of ASK, FSK and PSK with respect to probability of error.
5. (a) Define entropy of a discrete memoryless source and obtain the expression for it.  
(b) The probabilities of seven messages emitted by a source are  $\frac{1}{2}$ ,  $\frac{1}{4}$ ,  $\frac{1}{8}$ ,  $\frac{1}{16}$ ,  $\frac{1}{32}$ ,  $\frac{1}{64}$  and  $\frac{1}{64}$  respectively. Find the entropy and rate of information of the source.
6. (a) State the Shannon's source coding theorem and derive the expression for coding efficiency.  
(b) A discrete memoryless source produces symbols  $x_i$ , where,  $i= 0$  to  $5$  with the following probabilities:  $p(x_0)=0.1$ ;  $p(x_1)=0.2$ ;  $p(x_2)=0.15$ ;  $p(x_3)=0.09$ ;  $p(x_4)=0.20$ ;  $p(x_5)=0.26$ ; Design the Huffman code for the above source and find the coding efficiency.
7. (a) Describe the relationship between the generator polynomial  $g(x)$  and the parity-check polynomial  $h(x)$  of an  $(n, k)$  cyclic linear code.  
(b) For the  $(7, 4)$  symmetric hamming code, determine the generator matrix  $G$ , the parity-check matrix  $H$ , all the code words and the minimum distance of the code.
8. (a) What are the different methods of describing the structure of a convolutional encoder? Explain.  
(b) Assume a  $(2, 1)$  convolutional coder with constraint length 6. Draw the tree diagram and trellis diagram for the assumed coder.

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JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL COMMUNICATIONS**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) What are the two major sources of noise in a PCM system? Derive the expression for the output signal to quantization noise ratio in PCM?  
(b) Explain the need of predictor by DPCM to make voice and video transmission comparable to that of PCM.
2. (a) Draw the block diagrams of transmitter and receiver of a continuously variable step size adaptive delta modulation system and explain its working.  
(b) Describe the advantages, disadvantages and limitations of delta modulation.
3. (a) Describe the advantages and disadvantages of M-ary band pass signaling as compared to binary band pass signaling.  
(b) Explain the signal space diagram of 8-ary PSK and sketch the signal constellation.
4. (a) Explain transmission and reception of BPSK signal with suitable diagrams.  
(b) Derive an expression for the probability of symbol error for the BPSK scheme.
5. (a) Explain the joint and conditional entropies of a discrete memoryless channel with necessary expressions.  
(b) A source emits one of four messages every microsecond. The probabilities of these messages are 0.5, 0.3, 0.1 and 0.1. Messages are generated independently. Determine the entropy and rate of information generated by the source.
6. (a) Derive the expression for the channel capacity of a Gaussian channel.  
(b) Two binary symmetric channels one with a transition probability of 0.1 and the other with a transition probability of 0.2 are connected in cascade. Determine the equivalent channel.
7. (a) Draw the block diagram of an encoder for a linear (n, k) block code and explain its working.  
(b) A binary linear block code has a generator matrix ; Determine all its code words.
8. (a) What is meant by free distance of a convolutional code? How does it affect the number of errors that can be corrected and coding gain?  
(b) Draw the block diagram of a half rate convolutional encoder with constraint length 3. Determine the generator polynomial of the encoder.

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JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL COMMUNICATIONS**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Draw the block diagram of transmitter and receiver sections of differential PCM system and explain each block.  
(b) In a binary PCM system, the output signal to quantizing noise ratio is to be held to a minimum value of 40 dB. Determine the number of required levels and find the corresponding output signal-to-quantizing noise ratio.
2. (a) With a neat block diagram explain the principle of delta modulation and derive the expression for average output noise power in delta modulation.  
(b) What are the types of quantization errors occurring in delta modulation? Explain in detail.
3. (a) Draw the block diagram of a QPSK receiver and explain its working.  
(b) Describe the principle of OQPSK and write its advantages and disadvantages.
4. (a) Draw the block diagram of non-coherent BFSK receiver and explain its operation.  
(b) Derive the expression for probability of error for non-coherent BFSK.
5. (a) What is average information? Describe its properties.  
(b) A source emits seven messages with probabilities  $1/3, 1/3, 1/9, 1/9, 1/27, 1/27$  and  $1/27$  respectively. Find the entropy and rate of information of the source.
6. (a) What is a binary symmetric channel and derive the expression for its capacity?  
(b) A discrete memoryless source with alphabet  $s_0, s_1$  and  $s_2$  produces them with probabilities of 0.7, 0.2 and 0.1 respectively. Using Shannon-Fano algorithm devise and unambiguous code for the source output and determine its coding efficiency.
7. (a) Draw the block diagram of the syndrome calculator for an  $(n, k)$  cyclic code and explain its working.  
(b) A linear  $(n, k)$  block code has a generator matrix: ; Find all its code words, H matrix and minimum distance of the code.
8. (a) A particular convolutional code is described as an  $(n, k, L)$  code. What do these letters  $n, k$  and  $L$  represent? Explain.  
(b) The generators of a  $1/3$  rate convolutional code are:  $g_1=[1 \ 0 \ 0]$ ;  $g_2=[1 \ 0 \ 1]$  and  $g_3=[1 \ 1 \ 1]$ . Draw the encoder circuit and Trellis diagram corresponding to this code.

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Code No: R31042

**R10**

**Set No: 1**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL IC APPLICATIONS**  
(Com. to ECE, EIE, BME,ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Design a CMOS transistor circuit for 3-input AND gate. With the help of function table explain the circuit.  
(b) Define the term electro-static discharge (ESD) and explain how a CMOS device is destroyed.
2. a) Draw and explain the operation of transistor inverter with its transfer characteristics?  
b) What is schottky transistor? Why it is used in logic families?
3. a) Explain the design and analysis procedure of combinational circuit with suitable example.  
b) Using two 74x138 decoders design a 4 to 16 decoder.
4. a) Draw the circuit diagram of a barrel shifter which can shift 0,1,2& 3 bit positions area as per the control signals S1 and S2.  
b) What do you mean by carry propagation delay? Explain the method used for fast addition?
5. a) Design a excess-3 to decimal counter using 74x163.  
b) Define clock skew. Explain how it leads to incorrect output in synchronous circuits. Design one logic circuit that minimizes clock skew.
6. a) Design a 4-bit, 8-state ring counter using 74x194 IC.  
b) Draw and explain the operation of parallel-in parallel-out shift register.
7. a) With the help of logic diagram explain PAL16R8?  
b) What is Macro cell? Explain the structure of Macro cell used in the PAL ICs?
8. a) Explain the internal structure of 64Kx1 DRAM.  
b) What is decoding? Explain the necessity of two dimensional decoding mechanism in memories.

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**R10**

**Set No: 2**

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III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL IC APPLICATIONS**  
(Com. to ECE, EIE, BME, ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. a) Design a 4-input CMOS OR-AND-INVERTER gate. Draw the logic diagram and function table.  
b) Explain the effect of floating inputs on CMOS gate.
2. a) Draw the circuit diagram of two input LS-TTL NOR gate and explain its functional behavioural.  
b) Write a note on TTL families.
3. a) Draw the logic diagram of 74x157 and explain its operation.  
b) Explain briefly about code converters.
4. a) Explain the operation of Dual priority encoder and also give the pin description for the same ?  
b) Draw and explain the block diagram of n-bit parallel adder.
5. a) Design a mod 120 counter using 7490 and 7492 ICs.  
b) What do you mean by sequential circuit? Explain with the help of block diagram & give the comparisons between combinational and sequential circuits.
6. a) With the help of two shift registers design a 4-bit serial adder.  
b) How synchronous counters differ from asynchronous counter. Draw the complete timing diagram for the five-stage synchronous binary counter.
7. a) Design sequence detector to detect a sequence 1101 using suitable PLA. Give state diagram and state table.  
b) Draw and explain the structure and configuration of PALs?
8. a) Design an 8x4diode ROM using 74x138 for the following data starting from the first location B,2,4,F,A,D,F,E.  
b) Draw and explain the architecture of SDRAM.

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**DIGITAL IC APPLICATIONS**

(Com. to ECE, EIE, BME, ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. a) Draw a circuit diagram, functional table and logic symbol for a CMOS gate with two inputs A and B and an output Z where  $Z=0$  if  $A=0$  and  $B=1$  and  $Z=1$  otherwise.  
b) What is the difference between transition time and propagation delay? Explain these two parameters with reference to CMOS logic.
2. a) Draw and explain the operation of OR gate & AND gate using diode logic?  
b) Write a note on cascading of diode gates?
3. a) Design a 32 to 1 MUX using 74x151 and 74x139 decoders.  
b) Write a short note on parity generator and checker.
4. a) Draw the logic diagram of 74x283 IC and design a 24-bit ripple adder using the same IC.  
b) Explain the working of n-bit subtractor with the help of neat block diagram?
5. a) Design a switch debouncer circuit using 74x109 IC.  
b) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.
6. a) Draw the logic diagram of 74x194 IC and explain its operation.  
b) Explain how serial data communication is possible using 74x166 as transmitter and 74x164 as receiver.
7. With the help of logic diagram explain the function of PAL16R6. Explain how an 8-bit synchronous binary counter can be realized with this device.
8. a) Realize the logic function performed by 74x381 ROM.  
b) Draw and explain the block diagram of memory unit.

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III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**DIGITAL IC APPLICATIONS**

(Com. to ECE, EIE, BME, ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
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1. a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuit? Mention the typical values of a CMOS NAND gate.  
b) Write a note on unused CMOS inputs.
2. Explain about the salient features of schottky TTL family. Give typical values of various parameters. Compare this logic family with that of standard TTL family.
3. a) Give the logic diagram of 74x139. Explain with the help of truth table? Using this IC design the 3 to 8 decoder.  
b) Design a 3-bit comparator using three one bit comparators and logic gates.
4. a) Explain in detail about simple floating point encoder.  
b) Design a barrel shifter for 8-bit using 3 control inputs.
5. a) Draw the logic diagram of 74x174 IC and explain its operation.  
b) Explain the operation of a D-latch through suitable timing diagram for various possibilities of input.
6. a) Design a 8-bit universal parallel-in-serial-out shift register.  
b) What is ring counter? Draw and explain the general structure of LFSR counter.
7. a) Tabulate the PLA programmable table for the four Boolean functions listed below.  
$$A(x, y, z) = \sum m (0, 1, 2, 4, 6) \quad B(x, y, z) = \sum m (0, 2, 6, 7)$$
$$C(x, y, z) = \sum m (3, 6) \quad D(x, y, z) = \sum m (1, 3, 5, 7)$$
  
b) Give the comparison between fixed function IC approach, ASIC approach and PLD approach.
8. a) Explain how a 4x4 binary multiplier can be designed using 256x8 ROM.  
b) What is synchronous RAM? Explain the structure of synchronous RAM with the help of block diagram.

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Code No: R31044

**R10**

**Set No: 1**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015  
**ELECTRONIC MEASUREMENTS AND INSTRUMENTATIONS**

(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks  
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1. a) Define the following (i) Accuracy (ii) Resolution (iii) Precision (iv) sensitivity  
b) Explain the concept of error in measurement? [8+7]
2. a) Explain about the fixed and variable AF oscillators?  
b) Discuss about the standard signal generator with neat diagram? [8+7]
3. a) Draw and discuss the spectral displays of various modulations using Spectrum analyzer.  
b) Differentiate between the wave analyzer and a harmonic distortion analyzer? [7+8]
4. a) What are the advantages of dual trace over dual beam CROs for multiple trace?  
b) How is the vertical axis of an oscilloscope deflected? How does it differ from the horizontal axis? [7+8]
5. a) Write short notes on post deflection acceleration with respect to oscilloscope tube.  
b) What is the minimum distance,  $L$ , that will allow full deflection of 4cm at the oscilloscope screen with a deflection factor of 100v/cm and with an accelerating potential of 2000v? [8+7]
6. a) Give advantages and disadvantages of Maxwell's Inductance capacitance bridge  
b) The four arms of a Maxwell's capacitance bridge at balance are : arm ab, an unknown inductance  $L_1$ , having a resistance  $R_1$ , arm bc, a non-inductive resistance of 1000  $\Omega$ , arm cd, a capacitor of 0.5 $\mu$ F in parallel with a resistance of 1000 $\Omega$ , arm da, a resistance of 1000  $\Omega$ . Find the inductance  $L_1$  of arm ab. [8+7]
7. Write a short note on the following  
a) Piezo electric transducer      b) Thermocouples [8+7]
8. Write the measurement procedure the following physical parameters:  
a) Velocity      b) humidity      c) moisture [15]

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Code No: R31044

**R10**

**Set No: 2**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015  
**ELECTRONIC MEASUREMENTS AND INSTRUMENTATIONS**  
(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks  
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1. a) Define the sensitivity of a multimeter. Draw the block diagram of a simple multimeter and explain its operation?  
b) State the difference between accuracy and precision of a measurement? [10+5]
2. a) Explain with block diagram of an AF sine-square wave audio oscillator?  
b) Describe about the sweep generator with neat sketch? [8+7]
3. a) Where are spectrum analyzers commonly used?  
b) Draw the circuit diagram and explain the working of a heterodyne type wave analyzer? [5+10]
4. a) What is the specialty of a dual beam CRO?  
b) With the help of a circuit diagram explain the working of a triggered sweep generator? [5+10]
5. a) What effect does increasing the writing rate of an oscilloscope by increasing the accelerating potential have on the deflection sensitivity.  
b) How much voltage is required across two deflection plates separated by 1 cm to deflect an electron beam 1 degree, If the effective length of the deflection plates is 2cm and the accelerating potential is 1000 volts? [7+8]
6. a) Derive the general equations for balance of an a.c. bridge. Prove that "For balance in an a.c. bridge, both magnitude and phase have to be satisfied unlike a d.c. bridge where in only the magnitude condition is to be satisfied".  
b) Describe the sources and the null detectors that are used for a.c. bridges. [8+7]
7. Explain the following with neat sketch  
a) Resistance thermometers                      b) Thermistors [8+7]
8. Write the measurement procedure the following physical parameters:  
a) speed                      b) humidity                      c) proximity [15]

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Code No: R31044

**R10**

**Set No: 3**

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015  
**ELECTRONIC MEASUREMENTS AND INSTRUMENTATIONS**  
(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Why is a thermocouple measuring instrument classified as an RF instrument?  
b) Explain the following dynamic characteristics of an instrument?  
(i) Fidelity (ii) Dynamic error  
c) The value of a resistance is 4.7 k $\Omega$ , while measurement yield a value of 4.63 k $\Omega$  calculate (i) the relative accuracy of measurement and (ii) %accuracy [8+3+4]
2. a) Describe the function generator with neat block diagram? Explain the method of producing sine waves?  
b) How are broad band sweep frequencies generated using a sweep generator? [10+5]
3. What is meant by the distortion factor? How can this factor be measured? Explain with the help of a block diagram. [15]
4. a) Explain the significance of the following Lissajous figures:  
(i) Straight line (ii) Ellipse (iii) Circle.  
b) Discuss the following display modes of dual-trace CRO:  
(i) A and B chopped (ii) A and B Alternate.  
c) An electrically deflected CRT has a final anode voltage of 2000V and parallel deflecting plates 1.5cm long and 5mm apart. If the screen is 50cm from the centre of deflecting plates. Find (a) beam speed (b) the deflection sensitivity of the tube and (c) the deflection factor of the tube. [6+4+5]
5. a) State the application of oscilloscope?  
b) Differentiate between the active probe and passive probe? [5+10]
6. a) Describe in brief the different methods used for measurement of medium resistances  
b) The four arms of a wheat stone bridge have the following resistances : AB=100  $\Omega$ , BC=10 $\Omega$ , CD=4 $\Omega$ , DA=50 $\Omega$  A galvanometer of 20 ohms resistance is connected across BD. Calculate the current through the galvanometer when a potential difference of 10 volts is maintained across AC. [7+8]
7. Write a short note on the following  
a) Sensistors b) Thermocouples [7+8]
8. a) What are the four types of electrical pressure transducer and explain any one?  
b) State the objectives of data acquisition system? [8+7]

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Code No: R31044

R10

Set No: 4

JNT University Kakinada

III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**ELECTRONIC MEASUREMENTS AND INSTRUMENTATIONS**

(Com. to ECE, EIE)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. a) Differentiate between a series type ohmmeter and a shunt type ohmmeter?  
b) Calculate the value of the multiplier resistance on the 50 V range of a d.c voltmeter, that uses a 200  $\mu$ A meter movement with an internal resistance of 100  $\Omega$ . [10+5]
2. a) Discuss with the help of a neat circuit diagram the elements of a standard sweep generator. Draw the output waveform.  
b) Explain the working of random noise generator with neat diagram? [10+5]
3. a) With the help of a block diagram, explain an AF wave analyzer?  
b) State the applications of a spectrum analyzer? [9+6]
4. a) Draw the neat sketch of the CRT and explain the main components of it.  
b) Explain the electrostatic Focusing used in all CROs. [10+5]
5. a) What do you mean by multi trace with respect to oscilloscopes?  
b) With a neat block diagram explain the each block of a dual-trace oscilloscope. [5+10]
6. a) What are the different sources of errors in a.c. bridges?  
b) The arms of Five node bridge are as follows:  
arm ab : an unknown impedance ( $R_1, L_1$ ) in series with a non-inductive variable resistor  $r_1$   
arm bc : a non inductive resistor  $R_3 = 100 \Omega$   
arm cd : a non inductive resistor  $R_4 = 200 \Omega$   
arm da : a non inductive resistor  $R_2 = 250 \Omega$   
arm de : a non inductive variable resistor  $r$   
arm ec : a loss-less capacitor  $C = 1 \mu F$ , and arm be : a detector  
An a.c. supply is connected between a and c. Calculate the resistance and inductance  $R_1, L_1$ , when under balanced conditions  $r_1 = 43.1 \Omega$  and  $r = 229.7 \Omega$  [5+10]
7. a) Name some common types of strain gauges?  
b) What characteristics determine the size of the strain gauge?  
c) Explain the functioning of a foil type strain gauge. [5+5+5]
8. a) Explain about the data acquisition system with a neat sketch?  
b) Discuss the transducer used to measure humidity and explain the procedure of measurement? [8+7]

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Code No: R31043

R10

Set No: 1

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**LINEAR IC APPLICATIONS**  
(Com. to ECE,EIE, BME,ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) For a dual input, balanced output differential amplifier  $R_C=2.2\text{ K}\Omega$ ,  $R_E=4.7\text{ K}\Omega$ ,  $R_{S1}=R_{S2}=50\text{ }\Omega$ , the supply voltages are  $\pm 10\text{V}$ . The  $h_{fe}$  for the transistor is 50. Assume silicon transistor  $h_{ie}=1.4\text{ K}\Omega$ , determine the operating point values. Differential gain, common mode gain and CMRR.  
(b) Obtain the AC analysis of differential amplifier using h-parameters for dual input balanced output. [7+8]
2. (a) What is slew rate? Derive an equation for it.  
(b) Discuss the features of 741 op amp.  
(c) Define thermal drift and PSRR. [5+5+5]
3. (a) Draw and explain the operation of voltage to current converter with floating load.  
(b) Find  $R_1$  and  $R_f$  in the lossy integrator so that the peak gain is 20dB and gain is 3 dB down from its peak when  $\omega=10,000\text{ rad/sec}$ . use a capacitance of  $0.01\mu\text{F}$ . [7+8]
4. (a) Distinguish between comparator with the Schmitt trigger  
(b) Explain the hysteresis curve in Schmitt trigger.  
(c) Discuss the limitations of comparator. [7+4+4]
5. (a) Draw a twin T notch filter and obtain an equation for transfer function and plot the frequency response.  
(b) Design a fourth order butttterworth low pass filter having an upper cutoff frequency of 1KHz. [7+8]
6. (a) Discuss the applications of monostable multivibrator using 555 timer.  
(b) Give the block diagram of IC566 VCO and explain the operation. [7+8]
7. (a) Draw and explain the 1408 DAC and obtain the output voltage when the binary input word is 00000000,10000000 and 11111111.  
(b) Explain the various sources of errors in DAC . [8+7]
8. (a) Explain the performance characteristics of a sample and hold circuits.  
(b) Draw and explain the analog multiplier circuit. [8+7]

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Code No: R31043

R10

Set No: 2

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**LINEAR IC APPLICATIONS**  
(Com. to ECE,EIE, BME,ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Give the reasons for using level translator in an IC op amp.  
(b) An op amp has a differential gain of 80dB and CMRR of 95Db, if  $v_1=2\mu V$  and  $v_2=1.6\mu V$  then calculate the differential and common mode output values.  
(c) Discuss the effect of  $R_E$  to improve the CMRR. [5+5+5]
2. (a) Explain the external compensation techniques in detail.  
(b) Discuss the ideal op amp characteristics and draw and explain the ideal voltage transfer curve. [7+8]
3. (a) Draw the AC inverting amplifier and explain the operation.  
(b) What is an instrumentation amplifier? Discuss the applications of it in detail. [6+9]
4. (a) Draw and explain the full wave precision rectifier.  
(b) Design a triangular wave generator using a comparator block and an integrator block to oscillate at 4KHz and  $V_{o(p-p)}=7$  volts . use an op amp with  $\pm 15$  volts power supplies. Make necessary assumptions. [7+8]
5. (a) Draw a first order high pass Butterworth filter and analyze the circuit. [7+8]  
(b) (i) Design the band pass filter using OP amplifiers so that the  $f_c= 1$ KHz,  $Q=3$  and  $AF=10$ .  
(ii) Change the centre frequency to 1.5 KHz, keeping AF and the bandwidth constant.
6. (a) Explain the application of PLL as a frequency multiplier and AM demodulator.  
(b) Explain the application of monostable multivibrator as a linear ramp generator. [7+8]
7. (a) Explain the counter type A/D converter in detail. [8+7]  
(b) Draw a weighted resistor DAC and obtain the transfer characteristics of a 3 bit DAC.
8. (a) Explain the performance characteristics of a sample and hold circuits.  
(b) Draw and explain the analog multiplier circuit. [8+7]

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Code No: R31043

R10

Set No: 3

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**LINEAR IC APPLICATIONS**  
(Com. to ECE,EIE, BME,ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Draw the circuit of a single input balanced output and find voltage gain, input resistance and output resistance.  
(b) Explain the methods of realizing high input resistance. [8+7]
2. (a) Why are FET op amps better than BJT op amps.  
(b) A 741 C op amp is used as an inverting amplifier with a gain of 50. The voltage gain Vs frequency curve of 741C is flat up to 20KHz. What maximum peak to peak input signal can be applied without distorting the output.  
(c) Discuss the stability of an op amp. [5+4+6]
3. (a) Draw and explain the output waveforms of an ideal integrator circuit when the input is  
(i) sine wave (ii) step input (iii) square wave.  
(b) (i) design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to 1KHz.  
(ii) if a sine wave of 1V peak at 1000Hz is applied to the differentiator of part (i), draw its output waveform. [7+8]
4. (a) What is hysteresis? What parameters determine the hysteresis.  
(b) a Schmitt trigger with upper threshold level  $V_{UT}=0V$  and hysteresis width  $V_H=0.2V$  converts a 1KHz sine wave of amplitude 4V(p-p) to a square wave calculate the time duration of negative and positive portions of output waveforms.  
(c) Draw the transfer characteristics of an ideal and practical comparator. [5+5+5]
5. (a) Explain the various types of filters along with their frequency responses.  
(b) Design and obtain the frequency response of a band pass filter with  $f_L=400Hz$  and  $f_H=1KHz$  with a pass band gain of 1. [7+8]
6. (a) Design a frequency multiplier circuit using PLL IC 565 to multiply input frequency by 5 centre frequency by 50 KHz and power supply is  $\pm 10V$  DC. Find the lock and capture range frequency at output and state related tracking range and capture range limits for input.  
(b) Discuss the applications of VCO in detail. [7+8]
7. (a) What are the different sources of errors in DAC? Explain.  
(b) Draw an inverted R-2R ladder DAC? Show the division of current for digital input word 001? Explain. [6+9]
8. (a) Discuss the principle of a balanced modulator. Explain the balanced modulator using FET's  
(b) Write a short note on analog switches. [8+7]

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Code No: R31043

R10

Set No: 4

JNT University Kakinada  
III B.Tech. I Semester Regular/Supplementary Examinations, Dec - 2014/Jan -2015

**LINEAR IC APPLICATIONS**  
(Com. to ECE,EIE, BME,ECC)

Time: 3 Hours

Max Marks: 75

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Compare the four differential amplifier configurations .  
(b) Explain the operation of a differential amplifier with swamping resistors. [9+6]
2. (a) Draw the pin diagram of 741 op amp and discuss the ideal characteristics of a 741 op amp.  
(b) Discuss the internal compensation techniques in detail. [8+7]
3. (a) Design a practical integrator with a following specifications.  
(i) To integrate signals down to 200Hz and to produce a peak voltage of 0.1 V  
(ii) When the input is  $V_i = 10 \sin(2\pi \times 10^4 t)$  mV. Find the DC component at the output when the input is 10mVdc.  
(b) Explain the working of an op amp inverting amplifier and derive the expression for voltage gain. [8+7]
4. (a) Draw the circuit diagram and explain the basic antilog amplifier using diode and transistors.  
(b) What is the difference between the comparator and Schmitt trigger? Explain. [8+7]
5. (a) What is a notch filter. Draw the twin T notch filter and analyze the circuit and obtain the frequency response.  
(b) Determine the order of a low pass Butterworth filter that is to provide 40dB attenuation at  $\omega/\omega_h = 2$ .  
(c) Why are active filters preferred. [7+4+4]
6. (a) Draw and explain the functional diagram of 555 timer.  
(b) Discuss the role of a phase detector in PLL. And explain the digital phase detectors used in it. [7+8]
7. (a) Explain the R-2R ladder DAC for 3 bit DAC in detail.  
(b) Draw and explain the 8-bit DAC 1408 in detail. [8+7]
8. Write a short note on  
(a) Sample and hold amplifiers  
(b) Various applications of multipliers. [8+7]

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